Vishal Saxena

Curriculum Vitae

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Professional Preparation

1998–2002 **B.Tech., Electrical Engineering**, *Indian Institute of Technology (IIT) Madras*, Chennai, India.

2005–2007 **M.S., Electrical and Computer Engineering**, *Boise State University*, ID.
Thesis: Indirect Compensation Techniques for Multi-stage Operational Amplifiers

2007–2010 **Ph.D., Electrical and Computer Engineering**, *Boise State University*, ID.
Dissertation: Delta-Sigma Modulators for Wideband Analog to Digital Conversion

Professional Experience

Sep 2019–Present **Associate Professor**, *Electrical and Computer Engineering Dept., University of Delaware*.

Aug 2016– Aug 2019 **Micron Endowed Professor of Microelectronics and Associate Professor**, *Electrical and Computer Engineering Dept., University of Idaho*.

Aug 2016 **Associate Professor**, *Electrical and Computer Engineering Dept., Boise State University*.

Aug 2010–July 2016 **Assistant Professor**, *Electrical and Computer Engineering Dept., Boise State University*.

Spring 2010 **Special Instructor**, *Electrical and Computer Engineering Dept., Boise State University*.

2005 – 2009 **Research Assistant**, *Electrical and Computer Engineering Dept., Boise State University*.

Summer 2008 **Analog IC Design Intern**, *Lightwire Inc (now Cisco), Allentown, PA*.

Spring 2008 **Graduate Research Assistant**, *Electrical and Computer Engineering Dept., University of Texas at Austin*.

Summer 2006 **IC Design Intern**, *Micron Imaging (now Aptina Inc), Boise, ID*.

2002 – 2004 **Senior Hardware Design Engineer**, *Midas Communications Ltd., Chennai, India*.

Research and Scholarly Activities

Research Focus

Analog Integrated Circuits and Beyond-CMOS Computing

- **Hybrid CMOS Photonic integrated circuits**
  - CMOS Photonic ICs for energy-efficient Terabit/s rate optical interconnects
  - Hybrid Radio-frequency Photonic ICs
- **Neuromorphic Computing and Circuits for Edge-AI**
  - Neuromorphic Computing Circuits using emerging memory devices; in-memory computing
  - Spiking Neural Network Algorithms for enabling low-power AI at the Edge
- **High-Performance Analog ICs:**
  - High-speed data converters, Delta-sigma modulators, Sensor front-ends
  - Serial links: Phase-locked loops and clock-data recovery
  - Design automation of analog & mixed-signal ICs.

Honors and Awards

2019 **DARPA Young Faculty Award (YFA)**, Silicon Photonic enabled Reconfigurable Optical Analog Processor (SiROAP), $500,000.

2016 **Air Force Office of Sponsored Research (AFOSR) Young Investigator Award**, Realizing Large-Scale Integrated RF Photonic Signal Processing Systems, $360,000.

2015 **NSF CAREER Award**, Mixed-Signal Photonic Circuits for Energy-efficient High-speed Data Interfaces, $500,000.

2016 Idaho's **Accomplished under 40** Award (Idaho Business Review).

2013 Best Student Paper Award co-author for "Systematic Design of 10-bit 50MS/s Pipelined ADC," in IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED) 2013, Boise, ID

2006 Best Student Paper Award for "Indirect Feedback Compensation of CMOS Opamps," in IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED) 2006, Boise, ID

Publications

Peer-Reviewed Journal Publications

[J1] **Saxena, V.**, "Neuromorphic computing: From emerging devices to integrated circuits," *(invited) Journal of Vacuum Science & Technology (JVST)-B*, vol. 39, pp. 010 801 (1–19), 2021.

[J2] **Saxena, V.**, "Mixed-Signal Neuromorphic Computing Circuits using Hybrid CMOS-RRAM Integration," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 581–586, 2020.

[J3] R. Vaila, J. Chiasson, and **Saxena, V.**, "A Deep Unsupervised Feature Learning Spiking Neural Network with Binarized Classification Layers for EMNIST Classification," *IEEE Transactions on Emerging Topics in Computational Intelligence (TETCI)*, pp. 1–12, 2020.

[J4] M. J. Shawon and **Saxena, V.**, "Rapid Simulation of Photonic Integrated Circuits Using Verilog-A Compact Models," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 10, pp. 3331–3341, 2020.

[J5] **Saxena, V.**, X. Wu, I. Srivastava, and K. Zhu, "Towards neuromorphic learning machines using emerging memory devices with brain-like energy efficiency," *(invited) Special Issue CMOS Low Power Design, Journal of Low Power Electronics and Applications (JLPEA)*, vol. 8, no. 4, 2018.

[J6] X. Wu and **Saxena, V.**, "Dendritic Processing Enables Bio-Plausible Stochastic STDP in Compound Binary Synapse," *IEEE Transaction on Nanotechnology (TNANO)*, vol. 18, pp. 149–159, 2018.

[J7] K. Zhu and **Saxena, V.**, "From Design to Test: A High-Speed PRBS," *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*, vol. 26, no. 10, pp. 2099 – 2107, 2018.

[J8] K. Zhu and **Saxena, V.**, "Case Study of a Hybrid Optoelectronic Limiting Receiver," *IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers*, vol. 64, no. 10, pp. 2797 – 2805, 2017.

[J9] S. Balagopal, K. Zhu, X. Wu, and **Saxena, V.**, "Design-to-Test: A Low-Power, 1.25 GHz, Single-Bit Single-Loop Continuous-Time Modulator with 15 MHz Bandwidth and 60 dB Dynamic Range," *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 90, no. 3, pp. 625–638, 2017.

[J10] X. Wu, **Saxena, V.**, and K. Zhu, "Homogeneous Spiking Neuromorphic System for Real-World Pattern Recognition," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 5, no. 2, pp. 254 – 266, June 2015.

[J11] X. Wu, **Saxena, V.**, and K. Zhu, "A CMOS Spiking Neuron for Brain-Inspired Neural Networks with Resistive Synapses and In-Situ Learning," *IEEE Transactions on Circuits and Systems (TCAS) II: Express Briefs*, vol. 62, no. 11, pp. 1088–1092, 2015.

[J12] K. Zhu, **Saxena, V.**, X. Wu, and W. Kuang, "Design Considerations for Traveling-Wave Modulator Based CMOS Photonic Transmitters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 4, pp. 412 – 416, April 2015.

[J13] S. Balagopal and **Saxena, V.**, "A 1 GSps, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT Delta-Sigma ADC with 1.5 Cycle Quantizer Delay and Improved STF," *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 78, no. 2, pp. 275–286, 2014.

[J14] T. Tran, A. Rothenbuhler, E. H. Barney Smith, **Saxena, V.**, and K. A. Campbell, "Reconfigurable Threshold Logic Gates using Memristive Devices," *Journal of Low Power Electronics and Applications*, vol. 3, no. 2, pp. 174–193, 2013.

[J15] S. Balagopal and **Saxena, V.**, "A Low-Power Single-bit Continuous-time Delta-Sigma Converter with 92.5 Dynamic Range for Biomedical Applications," *Journal of Low Power Electronics and Applications*, vol. 2, no. 3, pp. 197–209, 2012.

Journal Manuscript Preprints or in Progress

[K1] M. J. Shawon and **Saxena, V.**, "Analysis of Trade-offs in RF Photonic Links based on Multi-Bias Tuning of Silicon Photonic Ring-Assisted Mach Zehnder Modulators," *under review in the IEEE Transactions on Circuits and Systems I: Regular Papers*, 2021.

[K2] R. Vaila, J. Chiasson, and **Saxena, V.**, "Deep Convolutional Spiking Neural Networks for Image Classification," *arXiv:1903.12272*.

Peer-Reviewed Conference Publications

[C1] **Saxena, V.**, "A Mixed-Signal Convolutional Neural Network Using Hybrid CMOS-RRAM Integration," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, 2021.

[C2] J. Shawon, Md. and **Saxena, V.**, "Analysis of RF Photonic Link using SiliconPhotonic Ring-Assisted Mach Zehnder Modulator," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020.

[C3] R. Vaila, J. Chiasson, and V. Saxena, ""continuous learning in a single-incremental-task scenario with spike features"," in *ICONS 2020: International Conference on Neuromorphic Systems*, 2020.

[C4] **Saxena, V.**, "A Process-Variation Robust RRAM-Compatible CMOS Neuron for Neuromorphic System-on-a-Chip," in *in proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, 2020.

[C5] R. Vaila, J. Chiasson, and V. Saxena, "Feature extraction using spiking convolutional neural networks," in *ACM Proceedings of the International Conference on Neuromorphic Systems (ICONS)*, 2019, p. 14.

[C6] J. Shawon, Md. and **Saxena, V.**, "Rapid Simulation of Photonic Integrated Circuits using Verilog-A Compact Models," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C7] R. Wang and **Saxena, V.**, "A CMOS Photonic Optical PAM-4 Transmitter Linearized using Three-Segment Ring Modulator," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C8] **Saxena, V.**, "High LRS-Resistance CMOS Memristive Synapses for Energy-Efficient Edge-AI and Neuromorphic System-on-a-Chip," in *(invited) IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C9] C. Li, K. Yu, J. Rhim, K. Zhu, N. Qi, **V. Saxena**, M. Fiorentino, and S. Palermo, "A 3D-Integrated 56 Gb/s NRZ/PAM4 Reconfigurable Segmented Mach-Zehnder Modulator based Si-photonics Transmitter," in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018.

[C10] J. Shawon, Md., R. Wang, and **Saxena, V.**, "Design and Modeling of Silicon Photonic Ring-Based Linearized RF-to-Optical Modulator," in *in the proceedings of IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

[C11] R. Wang, J. Shawon, Md., and **Saxena, V.**, "Design and Compact Modeling of Silicon-Photonic Coupling-Based Ring Modulators for Optical Interconnects," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

[C12] **Saxena, V.**, X. Wu, and K. Zhu, "Energy-Efficient CMOS Memristive Synapses for Mixed-Signal Neuromorphic System-on-a-Chip," in *IEEE International Symposium on Circuits & Systems (ISCAS)*, 2018.

[C13] **Saxena, V.**, X. Wu, I. Srivastava, and K. Zhu, "Towards Spiking Neuromorphic System-on-a-Chip with Bio-plausible Synapses using Emerging Devices," in *(invited) ACM NanoCom, Washington D.C.*, 2017.

[C14] R. Kehan, Z. Wang, X. Wu, and **Saxena, V.**, "Behavioral Modeling and Characterization of Silicon Photonic Mach-Zehnder Modulator," in *(invited) International Midwest Symposium on Circuits and System (MWSCAS), Boston*, Aug 2017.

[C15] K. Zhu, S. Balagopal, X. Wu, and **Saxena, V.**, "Realization of a 10 GHz PLL in IBM 130 nm SiGe BiCMOS Process for Optical Transmitter," in *proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, 2017.

[C16] X. Wu and **Saxena, V.**, "Enabling Bio-Plausible Multi-level STDP using CMOS Neurons with Dendrites and Bistable RRAMs," in *International Joint Conference on Neural Networks (IJCNN), Anchorage, Alaska*, July 2017.

[C17] J. Browning, **Saxena, V.**, D. Plumlee, T. Akinwande, M. Worthington, and B. Hay, "A phase-controlled magnetron using a modulated electron source," in *IEEE International Conference on Plasma Science (ICOPS)*. IEEE, 2016, pp. 1–1.

[C18] Z. Kehan, **Saxena, V.**, and X. Wu, "Modeling and Optimizing Bond Wire Packaging Interface in a Hybrid CMOS Photonic Traveling-Wave MZM Transmitter," in *proceedings of the IEEE System-on-a-Chip Conference (SOCC), Seattle*, 2016.

[C19] Z. Kehan, C. Li, N. Qi, K. Yu, R. Fiorentino, Marco Bluesoleil, and **Saxena, V.**, "Modeling of MZM-Based Photonic Link Power Budget," in *proceedings of the Optical Interconnects Conference 2016, San Diego*, 2016.

[C20] Z. Kehan, **Saxena, V.**, and X. Wu, "A Comprehensive Design Approach for a MZM Based PAM-4 Silicon Photonic Transmitter," in *International Midwest Symposium on Circuits and System (MWSCAS), Fort Collins, USA*, Aug 2015.

[C21] X. Wu, **Saxena, V.**, and Zhu, "A CMOS Spiking Neuron for Dense Memristor- Synapse Connectivity for Brain-Like Computing," in *International Joint Conference on Neural Networks (IJCNN), Killarney, Ireland*, July 2015.

[C22] Z. Kehan, **Saxena, V.**, X. Wu, and S. Balagopal, "Design Analysis of a 12.5 GHz PLL in 130 nm SiGe BiCMOS Process," in *submitted to IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2015.

[C23] Z. Kehan, **Saxena, V.**, and W. Kuang, "Compact Verilog-A Modeling of Silicon Traveling-Wave Modulator for Hybrid CMOS Photonic Circuit Design," in *proc. 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station*, 2014.

[C24] W. Xinyu, **Saxena, V.**, and K. A. Campbell, "Energy-efficient STDP-based learning circuits with memristor synapses," in *proc. SPIE Machine Intelligence and Bio-inspired Computation, Baltimore*, 2014.

[C25] Z. Kehan, S. Balagopal, and **Saxena, V.**, "Design of a 10-Gb/s Integrated Limiting Receiver for Silicon Photonics Interconnects," in *proc. 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus*, 2013.

[C26] S. Balagopal, Z. Kehan, and **Saxena, V.**, "Systematic Synthesis of Cascaded Continuous-time Delta-Sigma ADCs for Wideband Data Conversion," in *(invited) proc. 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus*, Aug 2013.

[C27] Z. Kehan, S. Balagopal, and **Saxena, V.**, "Systematic Design of a 10-bit Pipelined ADC," in *submitted to IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2013.

[C28] T. Tran, A. Rothenbuhler, E. Barney Smith, **Saxena, V.**, and K. Campbell, "Reconfigurable Threshold Logic gates using Memristive Devices," in *IEEE Subthreshold Microelectronics Conference, Waltham, MA*, 2012.

[C29] S. Balagopal and **Saxena, V.**, "Design of Wideband Continuous-Time Delta-Sigma ADCs Using Two-Step Quantizers," in *(invited) proc. 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise*, Aug 2012.

[C30] S. Balagopal and **Saxena, V.**, "A 1 GSps, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT Delta-Sigma ADC with 1.5 Cycle Quantizer Delay and Improved STF," in *proc. 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise*, Aug 2012.

[C31] R. Koppula, S. Balagopal, and **Saxena, V.**, "Multi-bit Continuous-time Delta-Sigma Modulator for Audio Applications," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2012.

[C32] G. VanAckern, R. J. Baker, A. J. Moll, and **Saxena, V.**, "On-Chip 3D Inductors using Thru-Wafer Vias," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2012.

[C33] R. M. R. Koppula, S. Balagopal, and **Saxena, V.**, "Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs," in *proceedings of IEEE System on Chip Conference (SOCC), Taipei, Taiwan*, Sep 2011.

[C34] **Saxena, V.**, S. Balagopal, and R. J. Baker, "Systematic Design of Three-Stage Opamps using Split-Length Compensation," in *(invited) proceedings of the 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, S. Korea*, 2011.

[C35] S. Balagopal, R. M. R. Koppula, and **Saxena, V.**, "Systematic Design of Multibit Continuous-time Delta-Sigma Modulators using Two-step Quantizers," in *(student paper contest) proceedings of the 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, S. Korea*, Aug 2011.

[C36] **Saxena, V.**, S. Balagopal, and H. Chen, "Reconfigurable Continuous-time Delta-Sigma ADCs for Sofware-Defined and Multistandard Radios," in *SDR'11 WinnComm*, 2011.

[C37] S. Balagopal and **Saxena, V.**, "A Low-Power Single-bit Continuous-time Delta-Sigma Converter with 92.5 dB Dynamic Range and design of Low-Voltage Delta-Sigma ADCs," in *IEEE/MITLL Subthreshold Microelectronics Conference, Boston*, Sep 2011.

[C38] S. Balagopal, R. M. Koppula, and **Saxena, V.**, "A 110uW Single-Bit Continuous-time Delta-Sigma Converter with 94.4dB Dynamic Range," in *proceedings of Dallas Workshop on Circuits and Systems (DCAS)*, Oct 2010.

[C39] **Saxena, V.** and R. J. Baker, "Indirect Compensation Techniques for Three-Stage Fully-Differential Opamps," in *(invited) proceedings of the 53rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2010.

[C40] **Saxena, V.** and R. J. Baker, "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," in *proceedings of the 53rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2010.

[C41] S. Gupta, **Saxena, V.**, K. Campbell, and R. Baker, "W-2W Current Steering DAC for Programming Phase Change Memory," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2009, pp. 59–62.

[C42] **Saxena, V.** and R. J. Baker, "Indirect Compensation Techniques for Three-Stage CMOS Opamps," in *proceedings of the 52nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2009, pp. 9–12.

[C43] **Saxena, V.**, K. Li, G. Zheng, and R. Baker, "A K-Delta-1-Sigma Modulator for Wideband Analog-to-Digital Conversion," in *proceedings of the 52nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2009, pp. 411–415.

[C44] **Saxena, V.** and R. J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors," in *proceedings of the 51st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2008, pp. 109–112.

[C45] **Saxena, V.** and R. J. Baker, "Indirect Feedback Compensation of CMOS Op-Amps," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 3–4.

[C46] K. Duvvada, **Saxena, V.**, and R. J. Baker, "High Speed Digital Input Buffer Circuits," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 11–12.

[C47] **Saxena, V.**, T. Plum, J. Jessing, and R. J. Baker, "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 17–18.

Book Chapters

[B1] **Saxena, V.** and R. J. Baker, *"Analog and Digital VLSI Design," Chapter 19 in the Fundamentals of Industrial Electronics, Wilamowski, B. M. and Irwin, J. D. (editors)*, edition ed. CRC Press, 2011.

[B2] **Saxena, V.**, *"High-performance CMOS Operational Amplifiers for Signal Processing," Chapter in the High Performance Analog and Power Management Circuit Design Techniques for Modern SoCs*, A. Garimella and P. M. Furth, Eds. Springer International Publishing AG, 2016.

[B3] **Saxena, V.**, *"Fully-Differential Operational Amplifiers Design and Simulation," Chapter in the High Performance Analog and Power Management Circuit Design Techniques for Modern SoCs*, A. Garimella and P. M. Furth, Eds. Springer International Publishing AG, 2016.

Conference Poster Presentations

[P1] R. Vaila, J. Chiasson, and V. Saxena, "Spiking CNNs with PYNN and NEURON," in *5th Neuro Inspired Computational Elements Workshop (NICE 2018)*, July 2018.

[P2] J. Shawon and V. Saxena, "Compact Modeling of Linearized CMOS Photonic Modulators for Millimeter-Wave Wireless," in *NSF mmWave RCN Workshop, Tucson*, 1 2018.

[P3] V. Saxena, "Linearized CMOS Photonic Modulators for Millimeter-Wave Wireless," in *NSF mmWave RCN Workshop, Madison*, July 2017.

[P4] V. Saxena, "Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing," in *5th Neuro Inspired Computational Elements Workshop (NICE 2017)*, July 2018.

[P5] V. Saxena, "Hybrid CMOS Photonic Integrated Circuits for Millimeter Wave Communication," in *NSF mmWave RCN Workshop*, July 2016.

[P6] V. Saxena, "Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing," in *SRC DARPA JUMP Workshop*, July 2017.

[P7] V. Molina and **Saxena, V.**, "Tunable Vernier Ring Filters in an Integrated CMOS Photonic Platform," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2016.

[P8] R. M. R. Koppula, S. Balagopal, and **Saxena, V.**, "Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, Apr 2011.

[P9] S. Stickel and **Saxena, V.**, "A Four-Phase Charge Pump with Power Supply Rejection Based Regulation," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2011.

Non-Peer-Reviewed Conference Publications

[D1] **Saxena, V.**, "Neuromorphic computing: From emerging devices to neuromorphic system-on-a-chip," *(invited abstract) AVS 66th International Symposium & Exhibition*, 2020.

[D2] **Saxena, V.**, X. Wu, and M. Mitkova, "Whitepaper: Addressing Challenges in Neuromorphic Computing with Memristive Synapses," in *under review in U.S. DoE Neuromorphic Computing Workshop, Oak Ridge National Laboratory*, July 2016.

[D3] **Saxena, V.** and R. J. Baker, "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," in *proceedings of the 4th Annual Austin Conference on Integrated Circuits and Systems*, 2009, pp. 24–25.

[D4] K. Li, **Saxena, V.**, G. Zheng, and R. Baker, "Full Feed-Forward K-Delta-1-Sigma Modulator," in *proceedings of the 4th Annual Austin Conference on Integrated Circuits and Systems*, 2009, pp. 26–27.

[D5] **Saxena, V.** and R. J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors," in *Indirect Compensation Technique for Low-Voltage Op-Amps,", proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, 2008.

Invention Disclosures

2014 V. Saxena, "Memory Controlled Circuit System And Apparatus", U.S. non-provisional patent application, 14/538,600

Research Grants Received

2020-2022 **DARPA Young Faculty Award (YFA)**, *Silicon Photonic enabled Reconfigurable Optical Analog Processor (SiROAP)*, (PI:Saxena), $500,000.

2018 - 2020 **NSF REU Supplement**, *Supplemental funding to the CAREER award*, (PI:Saxena), $8,000.

2015 - 2020 **NSF**, ***CAREER****: Mixed-Signal Photonics Interconnects for Energy-Efficient High-Performance Data Interfaces, with REU Supplement*, (PI:Saxena), $500,000.

2016 - 2019 **AFOSR**, ***Young Investigator Program (YIP) Award****: Realizing Large-scale Integrated RF Photonic Signal Processing Systems*, (PI:Saxena), $360,000.

2016 - 2019 **AFOSR**, *Phase-Controlled Magnetron Development* , (Co-PI:Saxena, PI:Browning), $448,572.

2014 - 2016 **NSF**, *SHF: Realizing Chip-scale Memristor-based Monolithically Integrated Spiking Neural Networks*, (Co-PIs: Saxena;Campbell, PI:Barney Smith), $500,000.

2014 - 2015 **Agilent Technologies University Research Award**, *Design of Silicon Photonic Filters*, (PI:Saxena), $40,000.

2013 - 2015 **NASA ISGC**, *Energy-efficient and Reliable Chip-scale Integrated Space Optical Communication Systems*, (PI:Saxena), $20,703.

Chip Fabrication Support

2021 **AFRL**, *Chip fabrication in Intel 22nm CMOS technology*, High-speed Optical Interconnects.

2014 **MOSIS**, *Chip fabrication in IBM 130nm CMOS technology*, valued at $48,000, Advanced Modulation Transceivers.

2013 **MOSIS**, *Chip fabrication in IBM 130nm CMOS technology*, valued at $48,000, High-speed Silicon Photonics Interconnects.

2012 **MOSIS**, *Chip fabrication in IBM 130nm CMOS technology*, valued at $48,000, High-speed Continuous-Time Delta-Sigma ADCs using Two-step Quantizers.

2011 **DARPA**, *130nm FD-SOI chip fabrication through MIT Lincoln Laboratories*, Chip fabrication grant.

Initiated and Directed Research Laboratories

Analog Mixed-Signal and Photonic IC Design Lab (AMPIC), *University of Delaware, 2019–present*,
Website: `https://www.eecis.udel.edu/~vsaxena/`.

Analog Mixed-Signal and Photonic IC Design Lab (AMPIC), *University of Idaho, 2016-2019*.

Analog and Mixed-Signal IC Design Lab (AMS), *Boise State University, 2010–2016*.

Media Coverage

2017 YouTube TEDx Talk "Smarter Computing Inspired by The Human Brain" in July 2017. `https://www.youtube.com/watch?v=b-HllGNA6QI`

2016 Selected for Accomplished Under 40 Award and listed in the Idaho Business Review's article "This year's Accomplished Under 40 show diversity, geographic reach" in Apr 2016.

2014 Quoted in the MIT Technology Review's article "A Brain-Inspired Chip Takes to the Sky" in the Nov 2014 issue.

2013 News articles covering the NSF CCF award, "Researchers Building a Computer Chip Based on the Human Brain" in Aug 2013.

Conference Tutorials

2020 "Neuromorphic Computing: Devices, Circuits and Algorithms" half-day tutorial at the IEEE ISCAS 2020 Conference at Seville, Spain.

2018 "Neuromorphic Computing: Devices, Circuits and Algorithms" half-day tutorial at the IEEE MWSCAS 2018 Conference at Windsor, Canada.

2018 "Neuromorphic Computing Circuits and Algorithms," half-day tutorial at the IEEE ICASSP 2018 Conference in Calgary, Canada.

2017 "Neuromorphic Computing Circuits using Emerging Devices," half-day tutorial at the IEEE MWSCAS 2017 Conference in Boston.

2016 "Oversampling Data Converter Design," two-hour tutorial at the IEEE SOCC 2017 Conference in Seattle.

2012 "Delta-Sigma ADC design: From System-level Design to Transistor-level Implementation," half-day tutorial presented at IEEE MWSCAS 2012 in Boise.

Conference Special Sessions

2020 Organized Special Session of invited contributions on "Mixed-Signal Circuits for Machine Learning and Edge-AI," at IEEE International Symposium on Circuits and Systems (ISCAS) 2020, Seville, Spain

2019 Organized Special Session of invited contributions on "Low-Power Devices, Circuits, Systems, and Algorithms for the Internet of Things," at IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) 2019, Dallas, TX

2018 Organized Special Session of invited contributions on "Mixed-Signal Circuits for Machine Learning," at IEEE ISCAS 2018, Florence, Italy

2017 Organized Special Session of invited contributions on "Low-Power Devices, Circuits, Systems, and Algorithms for the Internet of Things," at IEEE MWSCAS 2017, Boston, MA

2012 Organized Special Session of invited contributions on "Advances in Analog-to-Digital Converters," at IEEE MWSCAS 2016, College Station, TX

2012 Organized Special Session of invited contributions on "Advances in Delta-Sigma Data Converters," at IEEE MWSCAS 2017, Boise, ID

Invited Talks

2019 "Neuromorphic Computing: From Emerging Devices to Neuromorphic System-on-a-Chip," at AVS 66th International Symposium & Exhibition, Columbus, OH, Oct 26, 2019.

2019 "Neuromorphic Computing: From Emerging Devices to Neuromorphic System-on-a-Chip," at AVS 66th International Symposium & Exhibition, Columbus, OH, Oct 26, 2019.

2019 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at University of Delaware, Newark, DE.

2019 "Artificial Intelligence Devices at the Edge: Opportunities, Challenges and Implications," at UI Malcolm M. Renfrew Interdisciplinary Colloquium, Moscow, ID, Mar 26, 2019.

2019 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at Stevens Institute of Technology, Hoboken, NJ.

2018 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at Case Western Reserve University, Cleveland, OH.

2018 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at Florida International University, Miami, FL.

2017 "Neuromorphic Computing Circuits using Emerging Devices," at SUNY Poly Tech in Albany, NY.

2017 "Cross Physical-Layer Energy-efficient Links," Micron Inc Boise Campus, Aug 2017.

2017 "Smarter Computing Inspired by the Brain," TEDx UIdaho Event, May 2017.

2017 "Analog Spiking Neuromorphic Circuits using Emerging Memory devices," Micron Inc Boise Campus, Feb 2017.

2016 "Sustaining Integrated Circuits in the post Moores-scaling Era," University of Idaho, May 2016.

2015 "CMOS Photonics ICs for Energy-efficient Computing and Data Centers," Boise State Research Office, Mar 2015.

2014 "CMOS Photonics Integrated Circuits for Signal Processing," Agilent measurements Group, Santa Clara, Feb 2014.

2013 "Advances in Delta-Sigma Data Converters for Next-Generation Wireless Systems," University of Idaho Graduate Colloquium, Oct 2013.

Research Group

Graduate Students.

- Md Jubayer Shawon, PhD, (2017-current) RF Photonic IC Design
- Anuar Dorzhigulov, PhD, (2020-current) Neuromorphic IC Design
- Shubham Mishra, PhD, (2021-current) CMOS Photonics IC Design
- Ruthvik Vaila, PhD student at Boise State University (jointly co-advised with Dr. John Chiasson)

Undergraduate Students.

- Chase Lawrence, NSF REU Student. Spring 2021
- Susan Arnopolin, NSF REU Student. Fall 2020

Doctoral Students Graduated

2010-2014 **Sakkarapani Balagopal**, *"High-Speed Delta-Sigma Data Converters for Next-Generation Wireless Communication"*, now at Cirrus Logic, Austin, TX.

2012-2016 **Kehan Zhu**, *"Integrated Circuit Design for Hybrid Optoelectronic Interconnects"*, now at Maxim Integrated, Beaverton, OR.

2013-2016 **Xinyu Wu**, *"Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing"*, now at Micron Inc, Boise, ID.

2017-2020 **Rui Wang**, *finished by Prof. Herb Hess at U. Idaho, "Silicon Photonics: Overview, Building Block Modeling, Chip Design and its Driving Integrated Circuits Co-Design"*.

Masters Students Graduated

2011-2013 **Rajaram Mohan Roy Koppula**, *"A Mixed-Signal Design Flow Applied to a Continuous Time Delta Sigma Converter"*, now at Qualcomm, Phoenix, AZ.

2014-2016 **Virginia Molina**, *"RF Photonic Filter Design"*, now working on ASIC Design in UK.

2017-2019 **Md Jubayer Shawon**, *"RF Photonic IC Design"*, now pursuing PhD at U. Delaware.

Student Honors and Awards

(Only to show active involvement and support for students in academic and research honors and awards)

2019 **Md. Jubayer Shawon**.
Received the prestigious IEEE Solid State Circuits Society (SSCS) 2019 Student Travel Grant to attend International Solid State Circuits Conference (ISSCC) in San Francisco.

2018 **Rui Wang**.
Received the prestigious IEEE Solid State Circuits Society (SSCS) 2018 Student Travel Grant to attend International Solid State Circuits Conference (ISSCC) in San Francisco.

2014 **Kehan Zhu**.
Received the IEEE SSCS 2014 Student Travel Grant to attend ISSCC at San Francisco.

2013 **Kehan Zhu**.
Received the Best Paper Award at the IEEE WMED Conference 2013 in Boise.

2011 **Sakkarapani Balagopal**, *Saxena Group Graduate Researcher*.
Received an NSF sponsored travel grant to attend SDR'11 WinnComm conference in Washington DC.

2010 **Sakkarapani Balagopal**.
Received the IEEE SSCS 2011 Student Travel Grant to attend ISSCC at San Francisco.

Teaching

Course Site: `https://www.eecis.udel.edu/~vsaxena/pages/teaching.html`

Teaching at the University of Delaware:

Course#	Course Title	Semester	Credit Hours	Graduate Enrollment	Undergrad Enrollment
ELEG 309	Electronic Circuit Analysis (with Lab)	Spring 2021	4	0	55
ELEG 662	ECE Seminar	Spring 2021			
CPEG 4/624	Analog IC Design	Fall 2020	3	4	22
ELEG 309	Electronic Circuit Analysis (with Lab)	Spring 2020	4	0	56

Teaching at the University of Idaho:

Course#	Course Title	Semester	Credit Hours	Graduate Enrollment	Undergrad Enrollment
ECE 310	Microelectronic Circuits	Spring 2019	3	0	18
ECE 311	Microelectronic Circuits Lab	Spring 2019	1	0	18
ECE 4/545	VLSI Design	Spring 2019	3	8	15
ECE 4/513	Radio Frequency IC Design	Fall 2018	3	5	3
ECE 4/515	Analog IC Design	Fall 2018	3	3	0
ECE 4/513	Radio Frequency IC Design	Fall 2018	3	5	3
ECE 4/515	Analog IC Design	Fall 2018	3	3	0
ECE 4/504	PLL & Serial Link Design (EO)	Spring 2018	3	1	0
ECE 310	Microelectronic Circuits	Spring 2018	3	0	19
ECE 311	Microelectronic Circuits Lab	Spring 2018	1	0	19
ECE 4/515	Analog IC Design	Fall 2017	3	5	3
ECE 4/504	Deep Learning and SNNs (Co-taught)	Fall 2017	3	12	2
ECE 4/517	Mixed-Signal IC Design	Spring 2017	3	2	2
ECE 4/504	PLL & Serial Link Design	Fall 2017	3	5	0

Teaching at Boise State University:

Course#	Course Title	Semester	Credit Hours	Graduate Enrollment	Undergrad Enrollment
ECE 697	Delta-Sigma Data Converter Design	Spring 2010	3	4	0
ECE 4/510	Physical Integrated Circuit Design	Fall 2010	3	6	5
ECE 4/511	CMOS Analog IC Design	Spring 2011	3	9	0
ECE 310	Microelectronic Circuits	Fall 2011	3	0	18
ECE 310L	Microelectronic Circuits Lab	Fall 2011	1	0	18
ECE 4/510	Physical Integrated Circuit Design	Fall 2011	3	11	2
ECE 4/511	CMOS Analog IC Design	Spring 2012	3	11	0
ECE 614	Advanced Analog IC Design	Fall 2012	3	3	0
ECE 4/511	CMOS Analog IC Design	Spring 2013	3	5	5
ECE 4/518	PLL & Memory IC Design	Spring 2013	3	8	1
ECE 4/510	Physical Integrated Circuit Design	Fall 2013	3	14	2
ECE 615	Mixed-Signal IC Design	Fall 2013	3	4	0
ECE 4/511	CMOS Analog IC Design	Spring 2014	3	8	1
ECE 4/510	Digital Integrated Circuit Design	Fall 2014	3	19	2
ECE 614	Advanced Analog IC Design	Fall 2014	3	5	0
ECE 4/511	CMOS Analog IC Design	Spring 2015	3	9	3
ECE 4/518	PLL & Memory IC Design	Spring 2015	3	9	2
ECE 4/510	Digital Integrated Circuit Design	Fall 2015	3	22	2
ECE 310	Microelectronic Circuits	Fall 2015	3	0	23
ECE 615	Mixed-Signal IC Design	Spring 2016	3	5	0

Service

Institutional Service at UD

2019– Member: ECE Department Research Day Committee

2021– Member: ECE Department ABET Committee

2020–2021 Member: College of Engineering Undergraduate Recruitment Task Force

Past Institutional Service

2017-2019 Member: UI UAS Committee

2017-2019 Member: COE Curriculum Committee

2017-2019 Member: IRIC Safety Committee

2010–2016 Member: BSU University Cultural and Ethnic Diversity Board (CEDB)

2013–2016 Member: BSU Faculty Senate Diversity Committee

2010–2012 Chair (elected): BSU Faculty Senate Diversity Committee

2010–2016 Chair: ECE Department Committee for ABET Accreditation Outcome (a)

2011–12 Member: ECE Department Student Recruitment Committee

2013 Member: ECE Department Undergraduate Committee

2014–2015 Member: ECE Department Outreach and Recruitment Committee

2015–2016 Member: ECE Department Graduate Committee

2014–2015 Member: ECE Department Faculty Search Committee

2014 Member: University Search Committee for Executive Director for the STEM Institute

2010– Academic Advisor: ECE graduate and undergraduate students

Professional Service and Synergistic Activities

2014-2015, 2018-2019 **Associate Editor**, *IEEE Transaction on Circuits and Systems II: Express Briefs*.

2017– **VLSI Technical Committee Member**, *IEEE International Symposium on Circuits and Systems (ISCAS)*.

2015– **Conference Steering Committee Member**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*.

2020- **Editorial Board Member**, *Journal of Low-Power Electronics and Applications (JLPEA)*.

2013-2015 **Inaugural Chair**, *Boise chapter of IEEE Solid-State Circuits Society (SSCS)*.

2012 Local Arrangements Chair and Mixed-Signal Circuits Track Chair- IEEE Int. MWSCAS Conference at Boise

2010-2019 Advisory Committee - IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)

Professional Society Membership.

- Senior Member, Institute of Electrical and Electronics Engineers (IEEE)
- Member, IEEE Circuits and Systems Society (CASS)
- Member, IEEE Solid-State Circuits Society (SSCS)
- Member, Eta Kappa Nu (HKN) Honor Society for Electrical and Computer Engineers

Technical Program Committees.

- IEEE International Symposium on circuits and Systems (ISCAS) 2021, Daegu, S. Korea
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2020, Springville, MA
- IEEE International Symposium on circuits and Systems (ISCAS) 2020, Seville, Spain
- IEEE International Symposium on circuits and Systems (ISCAS) 2019, Sapporo, Japan
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2018, Windsor
- IEEE International Symposium on circuits and Systems (ISCAS) 2018, Florence, Italy
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2017, Boston
- IEEE Latin American Symposium on Circuits and Systems (LASCAS) 2015
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2013, Columbus
- IEEE Int. Conference on VLSI Design 2013
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2012, Boise

Journal Review.

- IEEE Transactions on Circuits and Systems-I: Regular Papers
- IEEE Transactions on Circuits and Systems-II: Express Briefs
- IEEE Transactions on VLSI Systems
- Frontiers in Nanotechnology
- Nature Electronics
- IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)
- IEEE Transactions Neural Networks and Learning Systems (TNNLS)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- Springer Analog Integrated Circuits & Signal Processing (ALOG)

Conference Review.

- IEEE International Symposium on Circuits and Systems (ISCAS)
- IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)
- IEEE International Symposium on Biomedical Circuits and Systems (BioCAS)
- IEEE Custom Integrated Circuits Conference (CICC)

Grants Review Panels.

- National Science Foundation (NSF)
- Department of Energy (DOE ASCR)
- Department of Defense (DOD AFOSR)

Graduate Student Committees – Student List

Thesis Committee Chair or Research Advisor

Md. Jubayer Shawon (PhD), Rui Wang (PhD), Milad Hmeda (PhD), Nathan Totorica (MS), Sakkarapani Balagopal (PhD), Zhu Kehan (PhD), Xinyu (Tomas) Wu (PhD), Virginia Molina (PhD), Kim Helper (MS), Rajaram Mohan Roy Koppula (MS)

MS Thesis Committee Member

Gary Vanakern, Kyle Campbell, Benjamin Millemon, Thanh Tran, Adrian Ruthenbuhler, Ross Butler, Kolton Drake

PhD Thesis Committee Member

Jun Guo, Ruthvik Vaila, Jim Hall, Mahesh Ailavajhala, Muhammad Rizwan Latif, Michael Pook, Uri Rogers, Xia Li, Steve Wald, Jared Barclay

MEngr Comprehensive Exam Committee Member

Shwetha Vure, Petru Sandor, Anshika Sharma, Cameron Weisman

PhD Comprehensive Exam Committee Member

Abdelrahman Hesham Elsayed Ahmed (University of British Columbia), Sakkarapani Balagopal, Kehan Zhu, Mahesh Ailavazhala, Michael Pook, Steve Wald, Vikram Patel, Danyal Mohamadi, Virginia Molina, Luka Daoud, Fady Hussain