Vishal Saxena

Curriculum Vitae

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Professional Preparation

1998–2002 **B.Tech., Electrical Engineering**, *Indian Institute of Technology (IIT) Madras*, Chennai, India.

2005–2007 **M.S., Electrical and Computer Engineering**, *Boise State University*, ID.
Thesis: Indirect Compensation Techniques for Multi-stage Operational Amplifiers

2007–2010 **Ph.D., Electrical and Computer Engineering**, *Boise State University*, ID.
Dissertation: Delta-Sigma Modulators for Wideband Analog to Digital Conversion

Professional Experience

Sep 2019– Present **Associate Professor**, *Electrical and Computer Engineering Dept., University of Delaware*.

Aug 2016– Aug 2019 **Micron Endowed Professor of Microelectronics and Associate Professor**, *Electrical and Computer Engineering Dept., University of Idaho*.

Feb 2016– Aug 2016 **Associate Professor with Tenure**, *Electrical and Computer Engineering Dept., Boise State University*.

Aug 2010–Feb 2016 **Assistant Professor**, *Electrical and Computer Engineering Dept., Boise State University*.

Spring 2010 **Special Instructor**, *Electrical and Computer Engineering Dept., Boise State University*.

2005 – 2009 **Research Assistant**, *Electrical and Computer Engineering Dept., Boise State University*.

Summer 2008 **Analog IC Design Intern**, *Lightwire Inc (now Cisco), Allentown, PA*.

Spring 2008 **Graduate Research Assistant**, *Electrical and Computer Engineering Dept., University of Texas at Austin*.

Summer 2006 **IC Design Intern**, *Micron Imaging (now Aptina Inc), Boise, ID*.

2002 – 2004 **Senior Hardware Design Engineer**, *Midas Communications Ltd., Chennai, India*.

Research and Scholarly Activities

Research Focus

Analog Integrated Circuits and Beyond-CMOS Computing

- **Hybrid CMOS Photonic integrated circuits** and modeling to *Harness Light to Transform IC Design*.
  - CMOS Photonic ICs for energy-efficient Terabit/s rate optical interconnects
  - Hybrid Radio-frequency and Millimeter-Wave Photonic ICs
  - Emerging applications such as Quantum Computing and Photonics for Machine Learning
- **Neuromorphic Computing and Circuits for Edge-AI**
  - Neuromorphic Computing Circuits using emerging memory devices; in-memory computing
  - Spiking Neural Network Algorithms for enabling low-power AI at the Edge
- **High-Performance Analog ICs:**
  - High-speed data converters, Delta-sigma modulators, Sensor front-ends
  - Serial links: Phase-locked loops and clock-data recovery

Honors and Awards

2019 **DARPA Young Faculty Award (YFA)**, Silicon Photonic enabled Reconfigurable Optical Analog Processor (SiROAP), up to $1,000,000.

2016 **Air Force Office of Sponsored Research (AFOSR) Young Investigator Award**, Realizing Large-Scale Integrated RF Photonic Signal Processing Systems, $360,000.

2015 **NSF CAREER Award**, Mixed-Signal Photonic Circuits for Energy-efficient High-speed Data Interfaces, $500,000.

2016 Idaho's **Accomplished under 40** Award (Idaho Business Review).

2013 Best Student Paper Award co-author for "Systematic Design of 10-bit 50MS/s Pipelined ADC," in IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED) 2013, Boise, ID

2006 Best Student Paper Award for "Indirect Feedback Compensation of CMOS Opamps," in IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED) 2006, Boise, ID

Publications

Peer-Reviewed Journal Publications

[J1] **Saxena, V.**, X. Wu, I. Srivastava, and K. Zhu, "Towards neuromorphic learning machines using emerging memory devices with brain-like energy efficiency," *(invited) Special Issue CMOS Low*

Power Design, Journal of Low Power Electronics and Applications (JLPEA), vol. 8, no. 4, 2018.

[J2] X. Wu and **Saxena, V.**, "Dendritic Processing Enables Bio-Plausible Stochastic STDP in Compound Binary Synapse," *IEEE Transaction on Nanotechnology (TNANO)*, vol. 18, pp. 149–159, 2018.

[J3] K. Zhu and **Saxena, V.**, "From Design to Test: A High-Speed PRBS," *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*, vol. 26, no. 10, pp. 2099 – 2107, 2018.

[J4] K. Zhu and **Saxena, V.**, "Case Study of a Hybrid Optoelectronic Limiting Receiver," *IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers*, vol. 64, no. 10, pp. 2797 – 2805, 2017.

[J5] S. Balagopal, K. Zhu, X. Wu, and **Saxena, V.**, "Design-to-Test: A Low-Power, 1.25 GHz, Single-Bit Single-Loop Continuous-Time Modulator with 15 MHz Bandwidth and 60 dB Dynamic Range," *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 90, no. 3, pp. 625–638, 2017.

[J6] X. Wu, **Saxena, V.**, and K. Zhu, "Homogeneous Spiking Neuromorphic System for Real-World Pattern Recognition," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 5, no. 2, pp. 254 – 266, June 2015.

[J7] X. Wu, **Saxena, V.**, and K. Zhu, "A CMOS Spiking Neuron for Brain-Inspired Neural Networks with Resistive Synapses and In-Situ Learning," *IEEE Transactions on Circuits and Systems (TCAS) II: Express Briefs*, vol. 62, no. 11, pp. 1088–1092, 2015.

[J8] K. Zhu, **Saxena, V.**, X. Wu, and W. Kuang, "Design Considerations for Traveling-Wave Modulator Based CMOS Photonic Transmitters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 4, pp. 412 – 416, April 2015.

[J9] S. Balagopal and **Saxena, V.**, "A 1 GSps, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT Delta-Sigma ADC with 1.5 Cycle Quantizer Delay and Improved STF," *Springer Journal of Analog Integrated Circuits and Signal Processing*, vol. 78, no. 2, pp. 275–286, 2014.

[J10] T. Tran, A. Rothenbuhler, E. H. Barney Smith, **Saxena, V.**, and K. A. Campbell, "Reconfigurable Threshold Logic Gates using Memristive Devices," *Journal of Low Power Electronics and Applications*, vol. 3, no. 2, pp. 174–193, 2013.

[J11] S. Balagopal and **Saxena, V.**, "A Low-Power Single-bit Continuous-time Delta-Sigma Converter with 92.5 Dynamic Range for Biomedical Applications," *Journal of Low Power Electronics and Applications*, vol. 2, no. 3, pp. 197–209, 2012.

Journal Manuscript Preprints or in Progress

[K1] R. Vaila, J. Chiasson, and **Saxena, V.**, "Deep Convolutional Spiking Neural Networks for Image Classification," *arXiv:1903.12272*.

[K2] J. Shawon, Md. and **Saxena, V.**, "Rapid Simulation of Photonic Integrated Circuits using Verilog-A Compact Models," *under review in IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers*, 2019.

[K3] **Saxena, V.**, "Neuromorphic computing: From emerging devices to integrated circuits," *(invited) Journal of Vacuum Science & Technology A*, 2020.

Peer-Reviewed Conference Publications

[C1] **Saxena, V.**, "A Process-variation Robust RRAM-Compatible CMOS Neuron for Neuromorphic System-on-a-Chip," in *under review in IEEE International Symposium on Circuits & Systems (ISCAS)*, 2019.

[C2] R. Vaila, J. Chiasson, and V. Saxena, "Feature extraction using spiking convolutional neural networks," in *Proceedings of the International Conference on Neuromorphic Systems*. ACM, 2019, p. 14.

[C3] J. Shawon, Md. and **Saxena, V.**, "Rapid Simulation of Photonic Integrated Circuits using Verilog-A Compact Models," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C4] R. Wang and **Saxena, V.**, "A CMOS Photonic Optical PAM-4 Transmitter Linearized using Three-Segment Ring Modulator," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C5] **Saxena, V.**, "High LRS-Resistance CMOS Memristive Synapses for Energy-Efficient Edge-AI and Neuromorphic System-on-a-Chip," in *(invited) IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2019.

[C6] C. Li, K. Yu, J. Rhim, K. Zhu, N. Qi, **V. Saxena**, M. Fiorentino, and S. Palermo, "A 3D-Integrated 56 Gb/s NRZ/PAM4 Reconfigurable Segmented Mach-Zehnder Modulator based Si-photonics Transmitter," in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018.

[C7] J. Shawon, Md., R. Wang, and **Saxena, V.**, "Design and Modeling of Silicon Photonic Ring-Based Linearized RF-to-Optical Modulator," in *in the proceedings of IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

[C8] R. Wang, J. Shawon, Md., and **Saxena, V.**, "Design and Compact Modeling of Silicon-Photonic Coupling-Based Ring Modulators for Optical Interconnects," in *IEEE Int. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

[C9] **Saxena, V.**, X. Wu, and K. Zhu, "Energy-Efficient CMOS Memristive Synapses for Mixed-Signal Neuromorphic System-on-a-Chip," in *IEEE International Symposium on Circuits & Systems (ISCAS)*, 2018.

[C10] **Saxena, V.**, X. Wu, I. Srivastava, and K. Zhu, "Towards Spiking Neuromorphic System-on-a-Chip with Bio-plausible Synapses using Emerging Devices," in *(invited) ACM NanoCom, Washington D.C.*, 2017.

[C11] R. Kehan, Z. Wang, X. Wu, and **Saxena, V.**, "Behavioral Modeling and Characterization of Silicon Photonic Mach-Zehnder Modulator," in *(invited) International Midwest Symposium on Circuits and System (MWSCAS), Boston*, Aug 2017.

[C12] K. Zhu, S. Balagopal, X. Wu, and **Saxena, V.**, "Realization of a 10 GHz PLL in IBM 130 nm SiGe BiCMOS Process for Optical Transmitter," in *proc. of the IEEE International Symposium on Circuits & Systems (ISCAS)*, 2017.

[C13] X. Wu and **Saxena, V.**, "Enabling Bio-Plausible Multi-level STDP using CMOS Neurons with Dendrites and Bistable RRAMs," in *International Joint Conference on Neural Networks (IJCNN), Anchorage, Alaska*, July 2017.

[C14] J. Browning, **Saxena, V.**, D. Plumlee, T. Akinwande, M. Worthington, and B. Hay, "A phase-controlled magnetron using a modulated electron source," in *IEEE International Conference on Plasma Science (ICOPS)*. IEEE, 2016, pp. 1–1.

[C15] Z. Kehan, **Saxena, V.**, and X. Wu, "Modeling and Optimizing Bond Wire Packaging Interface in a Hybrid CMOS Photonic Traveling-Wave MZM Transmitter," in *proceedings of the IEEE System-on-a-Chip Conference (SOCC), Seattle*, 2016.

[C16] Z. Kehan, C. Li, N. Qi, K. Yu, R. Fiorentino, Marco Bluesoleil, and **Saxena, V.**, "Modeling of MZM-Based Photonic Link Power Budget," in *proceedings of the Optical Interconnects Conference 2016, San Diego*, 2016.

[C17] Z. Kehan, **Saxena, V.**, and X. Wu, "A Comprehensive Design Approach for a MZM Based PAM-4 Silicon Photonic Transmitter," in *International Midwest Symposium on Circuits and System (MWSCAS), Fort Collins, USA*, Aug 2015.

[C18] X. Wu, **Saxena, V.**, and Zhu, "A CMOS Spiking Neuron for Dense Memristor- Synapse Connectivity for Brain-Like Computing," in *International Joint Conference on Neural Networks (IJCNN), Killarney, Ireland*, July 2015.

[C19] Z. Kehan, **Saxena, V.**, X. Wu, and S. Balagopal, "Design Analysis of a 12.5 GHz PLL in 130 nm SiGe BiCMOS Process," in *submitted to IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2015.

[C20] Z. Kehan, **Saxena, V.**, and W. Kuang, "Compact Verilog-A Modeling of Silicon Traveling-Wave Modulator for Hybrid CMOS Photonic Circuit Design," in *proc. 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station*, 2014.

[C21] W. Xinyu, **Saxena, V.**, and K. A. Campbell, "Energy-efficient STDP-based learning circuits with memristor synapses," in *proc. SPIE Machine Intelligence and Bio-inspired Computation, Baltimore*, 2014.

[C22] Z. Kehan, S. Balagopal, and **Saxena, V.**, "Design of a 10-Gb/s Integrated Limiting Receiver for Silicon Photonics Interconnects," in *proc. 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus*, 2013.

[C23] S. Balagopal, Z. Kehan, and **Saxena, V.**, "Systematic Synthesis of Cascaded Continuous-time Delta-Sigma ADCs for Wideband Data Conversion," in *(invited) proc. 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus*, Aug 2013.

[C24] Z. Kehan, S. Balagopal, and **Saxena, V.**, "Systematic Design of a 10-bit Pipelined ADC," in *submitted to IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2013.

[C25] T. Tran, A. Rothenbuhler, E. Barney Smith, **Saxena, V.**, and K. Campbell, "Reconfigurable Threshold Logic gates using Memristive Devices," in *IEEE Subthreshold Microelectronics Conference, Waltham, MA*, 2012.

[C26] S. Balagopal and **Saxena, V.**, "Design of Wideband Continuous-Time Delta-Sigma ADCs Using Two-Step Quantizers," in *(invited) proc. 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise*, Aug 2012.

[C27] S. Balagopal and **Saxena, V.**, "A 1 GSps, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT Delta-Sigma ADC with 1.5 Cycle Quantizer Delay and Improved STF," in *proc. 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise*, Aug 2012.

[C28] R. Koppula, S. Balagopal, and **Saxena, V.**, "Multi-bit Continuous-time Delta-Sigma Modulator for Audio Applications," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2012.

[C29] G. VanAckern, R. J. Baker, A. J. Moll, and **Saxena, V.**, "On-Chip 3D Inductors using Thru-Wafer Vias," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2012.

[C30] R. M. R. Koppula, S. Balagopal, and **Saxena, V.**, "Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs," in *proceedings of IEEE System on Chip Conference (SOCC), Taipei, Taiwan*, Sep 2011.

[C31] **Saxena, V.**, S. Balagopal, and R. J. Baker, "Systematic Design of Three-Stage Opamps using Split-Length Compensation," in *(invited) proceedings of the 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, S. Korea*, 2011.

[C32] S. Balagopal, R. M. R. Koppula, and **Saxena, V.**, "Systematic Design of Multibit Continuous-time Delta-Sigma Modulators using Two-step Quantizers," in *(student paper contest) proceedings of the 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, S. Korea*, Aug 2011.

[C33] **Saxena, V.**, S. Balagopal, and H. Chen, "Reconfigurable Continuous-time Delta-Sigma ADCs for Sofware-Defined and Multistandard Radios," in *SDR'11 WinnComm*, 2011.

[C34] S. Balagopal and **Saxena, V.**, "A Low-Power Single-bit Continuous-time Delta-Sigma Converter with 92.5 dB Dynamic Range and design of Low-Voltage Delta-Sigma ADCs," in *IEEE/MITLL Subthreshold Microelectronics Conference, Boston*, Sep 2011.

[C35] S. Balagopal, R. M. Koppula, and **Saxena, V.**, "A 110uW Single-Bit Continuous-time Delta-Sigma Converter with 94.4dB Dynamic Range," in *proceedings of Dallas Workshop on Circuits and Systems (DCAS)*, Oct 2010.

[C36] **Saxena, V.** and R. J. Baker, "Indirect Compensation Techniques for Three-Stage Fully-Differential Opamps," in *(invited) proceedings of the 53rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2010.

[C37] **Saxena, V.** and R. J. Baker, "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," in *proceedings of the 53rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2010.

[C38] S. Gupta, **Saxena, V.**, K. Campbell, and R. Baker, "W-2W Current Steering DAC for Programming Phase Change Memory," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2009, pp. 59–62.

[C39] **Saxena, V.** and R. J. Baker, "Indirect Compensation Techniques for Three-Stage CMOS Op-amps," in *proceedings of the 52nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2009, pp. 9–12.

[C40] **Saxena, V.**, K. Li, G. Zheng, and R. Baker, "A K-Delta-1-Sigma Modulator for Wideband Analog-to-Digital Conversion," in *proceedings of the 52nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2009, pp. 411–415.

[C41] **Saxena, V.** and R. J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors," in *proceedings of the 51st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2008, pp. 109–112.

[C42] **Saxena, V.** and R. J. Baker, "Indirect Feedback Compensation of CMOS Op-Amps," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 3–4.

[C43] K. Duvvada, **Saxena, V.**, and R. J. Baker, "High Speed Digital Input Buffer Circuits," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 11–12.

[C44] **Saxena, V.**, T. Plum, J. Jessing, and R. J. Baker, "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," in *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2006, pp. 17–18.

Book Chapters

[B1] **Saxena, V.** and R. J. Baker, *"Analog and Digital VLSI Design," Chapter 19 in the Fundamentals of Industrial Electronics, Wilamowski, B. M. and Irwin, J. D. (editors)*, edition ed. CRC Press, 2011.

[B2] **Saxena, V.**, *"High-performance CMOS Operational Amplifiers for Signal Processing," Chapter in the High Performance Analog and Power Management Circuit Design Techniques for*

Modern SoCs, A. Garimella and P. M. Furth, Eds. Springer International Publishing AG, 2016.

[B3] **Saxena, V.**, *"Fully-Differential Operational Amplifiers Design and Simulation," Chapter in the High Performance Analog and Power Management Circuit Design Techniques for Modern SoCs*, A. Garimella and P. M. Furth, Eds. Springer International Publishing AG, 2016.

Conference Poster Presentations

[P1] R. Vaila, J. Chiasson, and V. Saxena, "Spiking CNNs with PYNN and NEURON," in *5th Neuro Inspired Computational Elements Workshop (NICE 2018)*, July 2018.

[P2] J. Shawon and V. Saxena, "Compact Modeling of Linearized CMOS Photonic Modulators for Millimeter-Wave Wireless," in *NSF mmWave RCN Workshop, Tucson*, 1 2018.

[P3] V. Saxena, "Linearized CMOS Photonic Modulators for Millimeter-Wave Wireless," in *NSF mmWave RCN Workshop, Madison*, July 2017.

[P4] V. Saxena, "Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing," in *5th Neuro Inspired Computational Elements Workshop (NICE 2017)*, July 2018.

[P5] V. Saxena, "Hybrid CMOS Photonic Integrated Circuits for Millimeter Wave Communication," in *NSF mmWave RCN Workshop*, July 2016.

[P6] V. Saxena, "Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing," in *SRC DARPA JUMP Workshop*, July 2017.

[P7] V. Molina and **Saxena, V.**, "Tunable Vernier Ring Filters in an Integrated CMOS Photonic Platform," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2016.

[P8] R. M. R. Koppula, S. Balagopal, and **Saxena, V.**, "Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, Apr 2011.

[P9] S. Stickel and **Saxena, V.**, "A Four-Phase Charge Pump with Power Supply Rejection Based Regulation," in *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, 2011.

Non-Peer-Reviewed Conference Publications

[D1] **Saxena, V.**, "Neuromorphic computing: From emerging devices to neuromorphic system-on-a-chip," *(invited abstract) AVS 66th International Symposium & Exhibition*, 2020.

[D2] **Saxena, V.**, X. Wu, and M. Mitkova, "Whitepaper: Addressing Challenges in Neuromorphic Computing with Memristive Synapses," in *under review in U.S. DoE Neuromorphic Computing Workshop, Oak Ridge National Laboratory*, July 2016.

[D3] **Saxena, V.** and R. J. Baker, "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," in *proceedings of the 4th Annual Austin Conference on Integrated Circuits and Systems*, 2009, pp. 24–25.

[D4] K. Li, **Saxena, V.**, G. Zheng, and R. Baker, "Full Feed-Forward K-Delta-1-Sigma Modulator," in *proceedings of the 4th Annual Austin Conference on Integrated Circuits and Systems*, 2009, pp. 26–27.

[D5] **Saxena, V.** and R. J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors," in *Indirect Compensation Technique for Low-Voltage Op-Amps,", proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, 2008.

Invention Disclosures

2014 V. Saxena, "Memory Controlled Circuit System And Apparatus", U.S. non-provisional patent application, 14/538,600

Research Grants Received

2019-2022 **DARPA Young Faculty Award (YFA)**, *Silicon Photonic enabled Reconfigurable Optical Analog Processor (SiROAP)*, (PI:Saxena), $500,000.

2018 - 2020 **NSF REU Supplement**, *Supplemental funding to the CAREER award*, (PI:Saxena), $8,000.

2015 - 2020 **NSF**, ***CAREER****: Mixed-Signal Photonics Interconnects for Energy-Efficient High-Performance Data Interfaces, with REU Supplement*, (PI:Saxena), $500,000.

2016 - 2019 **AFOSR**, ***Young Investigator Program (YIP) Award****: Realizing Large-scale Integrated RF Photonic Signal Processing Systems*, (PI:Saxena), $360,000.

2016 - 2019 **AFOSR**, *Phase-Controlled Magnetron Development* , (Co-PI:Saxena, PI:Browning), $448,572.

2014 - 2016 **NSF**, *SHF: Realizing Chip-scale Memristor-based Monolithically Integrated Spiking Neural Networks*, (Co-PIs: Saxena;Campbell, PI:Barney Smith), $500,000.

2014 - 2015 **Agilent Technologies University Research Award**, *Design of Silicon Photonic Filters*, (PI:Saxena), $40,000.

2013 - 2015 **NASA ISGC**, *Energy-efficient and Reliable Chip-scale Integrated Space Optical Communication Systems*, (PI:Saxena), $20,703.

Internal Research Grants

2012 - 2014 **BSU ECE Research Stimulus Grant**, *Integrated CMOS Photonics Circuits and Systems for Next-Generation Interconnects*, (PI:Saxena; Co-PIs:Wan Kuang), $75,000.

2012 - 2014 **BSU ECE Research Stimulus Grant**, *Integrated Neuromorphic Circuits using Chalcogenide Memristors*, (Neuromorphic Computing Team: Saxena; Campbell; Barney Smith), $73,600.

2012 - 2014 **BSU ECE Research Stimulus Grant**, *Study of Inductively Coupled Microplasma Devices*, (PI:Browning; Co-PIs:Saxena, Plumlee), $71,460.

Chip Fabrication Support

2014 **MOSIS**, *Chip fabrication in IBM 130nm CMOS technology*, valued at $48,000, Advanced Modulation Transceivers.

2013 **MOSIS**, *Chip fabrication in IBM 130nm CMOS technology*, valued at $48,000, High-speed Silicon Photonics Interconnects.

2012 **MOSIS**, *Chip fabrication in IBM 130nm CMOS technology*, valued at $48,000, High-speed Continuous-Time Delta-Sigma ADCs using Two-step Quantizers.

2011 **DARPA**, *130nm FD-SOI chip fabrication through MIT Lincoln Laboratories*, Chip fabrication grant.

Conference Tutorials

2018 "Neuromorphic Computing: Devices, Circuits and Algorithms" half-day tutorial at the IEEE MWSCAS 2018 Conference at Windsor, Canada.

2018 "Neuromorphic Computing Circuits and Algorithms," half-day tutorial at the IEEE ICASSP 2018 Conference in Calgary, Canada.

2017 "Neuromorphic Computing Circuits using Emerging Devices," half-day tutorial at the IEEE MWSCAS 2017 Conference in Boston.

2016 "Oversampling Data Converter Design," two-hour tutorial at the IEEE SOCC 2017 Conference in Seattle.

2012 "Delta-Sigma ADC design: From System-level Design to Transistor-level Implementation," half-day tutorial presented at IEEE MWSCAS 2012 in Boise.

Invited Talks

2019 "Neuromorphic Computing: From Emerging Devices to Neuromorphic System-on-a-Chip," at AVS 66th International Symposium & Exhibition, Columbus, OH, Oct 26, 2019.

2019 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at University of Delaware, Newark, DE.

2019 "Artificial Intelligence Devices at the Edge: Opportunities, Challenges and Implications," at UI Malcolm M. Renfrew Interdisciplinary Colloquium, Moscow, ID, Mar 26, 2019.

2019 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at Stevens Institute of Technology, Hoboken, NJ.

2018 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at Case Western Reserve University, Cleveland, OH.

2018 "Sustaining Advances in Integrated Circuits in the post CMOS-Scaling Era," at Florida International University, Miami, FL.

2017 "Neuromorphic Computing Circuits using Emerging Devices," at SUNY Poly Tech in Albany, NY.

2017 "Cross Physical-Layer Energy-efficient Links," Micron Inc Boise Campus, Aug 2017.

2017 "Smarter Computing Inspired by the Brain," TEDx UIdaho Event, May 2017.

2017 "Analog Spiking Neuromorphic Circuits using Emerging Memory devices," Micron Inc Boise Campus, Feb 2017.

2016 "Sustaining Integrated Circuits in the post Moores-scaling Era," University of Idaho, May 2016.

2015 "CMOS Photonics ICs for Energy-efficient Computing and Data Centers," Boise State Research Office, Mar 2015.

2014 "CMOS Photonics Integrated Circuits for Signal Processing," Agilent measurements Group, Santa Clara, Feb 2014.

2013 "Advances in Delta-Sigma Data Converters for Next-Generation Wireless Systems," University of Idaho Graduate Colloquium, Oct 2013.

Research Group

Graduate Students.

- Md Jubayer Shawon, PhD, (2017-current) RF Photonic IC Design
- Rui Wang, PhD, (2017-current) CMOS Photonic Interconnects
- Ruthvik Vaila, PhD student at Boise State (jointly co-advised with Dr. John Chiasson)

Doctoral Students Graduated

2010-2014 **Sakkarapani Balagopal**, *"High-Speed Delta-Sigma Data Converters for Next-Generation Wireless Communication"*, now at Cirrus Logic, Austin, TX.

2012-2016 **Kehan Zhu**, *"Integrated Circuit Design for Hybrid Optoelectronic Interconnects"*, now at Maxim Integrated, Beaverton, OR.

2013-2016 **Xinyu Wu**, *"Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-Inspired Cognitive Computing"*, now at Micron Inc, Boise, ID.

Masters Students Graduated

2011-2013 **Rajaram Mohan Roy Koppula**, *"A Mixed-Signal Design Flow Applied to a Continuous Time Delta Sigma Converter"*, now at Qualcomm, Phoenix, AZ.

2014-2016 **Virginia Molina**, *"RF Photonic Filter Design"*, now working on ASIC Design in UK.

2017-2019 **Md Jubayer Shawon**, *"RF Photonic IC Design"*, now pursuing PhD at U. Delaware.

Service

Professional Service and Synergistic Activities

2014–2015, 2018– **Associate Editor**, *IEEE Transaction on Circuits and Systems II: Express Briefs*.

2017– **VLSI Technical Committee Member**, *IEEE International Symposium on Circuits and Systems (ISCAS)*.

2015– **Conference Steering Committee Member**, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*.

2013-2015 **Inaugural Chair**, *Boise chapter of IEEE Solid-State Circuits Society (SSCS)*.

2012 Local Arrangements Chair and Mixed-Signal Circuits Track Chair- IEEE Int. MWSCAS Conference at Boise

2010-2019 Advisory Committee - IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)

Technical Program Committees.

- IEEE International Symposium on circuits and Systems (ISCAS) 2019, Sapporo, Japan
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2018, Windsor
- IEEE International Symposium on circuits and Systems (ISCAS) 2018, Florence, Italy
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2017, Boston
- IEEE Latin American Symposium on Circuits and Systems (LASCAS) 2015
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2013, Columbus
- IEEE Int. Conference on VLSI Design 2013
- IEEE Int. Midwest Symposium on circuits and Systems (MWSCAS) 2012, Boise

Professional Society Membership.

- Institute of Electrical and Electronics Engineers (IEEE)
- IEEE Circuits and Systems Society (CASS)
- IEEE Solid-State Circuits Society (SSCS)
- Eta Kappa Nu (HKN) Honor Society for Electrical and Computer Engineers