Chengmo Yang

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Research Interests:

My research interests lie in the broad areas of embedded systems, design automation, and computer architecture, with a particular focus on improving security, reliability, non-volatility, and energy efficiency of embedded systems, cyber physical systems, and Internet-of-Things.

Career Highlights:

- Won the NSF career award at first try.
- Received five grants (all as PI) with a total of $1.02M amount.
- Received one best paper award and three best paper nominations.
- Published 73 papers in IEEE/ACM transactions or first-tier conferences. Another 7 papers are currently under review.
- Supervising/supervised eleven PhD students who together have won 16 awards.
- Recruited three female PhD students and serving as the faculty advisor of the IEEE WIE affinity group in the University of Delaware.
- Mentored 20 undergraduate students for various research projects. Of them one is female, three are African American, and one has a disability.
- Organized an annual "robot world cup competition" four times for ECE undergraduate students.

Education:

- **Doctor of Philosophy** 09/2010
  Department of Computer Science and Engineering, University of California, San Diego
  Thesis: Tackling Computation Uncertainty through Fine-grained and Predictable Execution Adaptivity in Multicore Systems (Advisor: Alex Orailoglu)
- **Master of Science** 09/2005
  Department of Computer Science and Engineering, University of California, San Diego
- **Bachelor of Science** 07/2003
  Department of Microelectronics, Peking University, China

Professional Experience:

- **Associate Professor** 09/2016 – Present
  Department of Electrical and Computer Engineering, University of Delaware

- **Senior Visiting Scholar** 02/2017 – 08/2017
  Department of Electrical Engineering, Tsinghua University, China
- **Assistant Professor** 09/2010 – 08/2016
  Department of Electrical and Computer Engineering, University of Delaware
- **Graduate Research Assistant** 09/2004 – 08/2010
  Department of Computer Science and Engineering, University of California, San Diego
- **Graduate Teaching Assistant** 06/2004 – 08/2010
  Department of Computer Science and Engineering, University of California, San Diego
- **Engineer Intern** Summer 2007, Summer 2008
  Broadcom Corporation, San Diego, CA
  Developed a behavior-level cycle accurate simulation and testing environment based on RTL description of application-specific SoCs
- **Engineer Intern** Summer 2006
  Mindspeed Technologies, Newport Beach, CA
  Developed a cycle accurate configurable system-level simulator for an application-specific SoC for voice processing products
- **Undergraduate Research Assistant** 02/2002 – 06/2003
  Department of Computer Science, Peking University, China
  Worked on instruction-level simulation & verification for SoCs, as well as logic synthesis & static timing analysis for SoCs

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Honors and Awards:

- 1st place in Worldwide Cyber Security Awareness Week (CSAW) Embedded System Challenge Competition 2018
- Best paper nomination in Design Automation Conference (DAC) 2017
- 2nd place in Worldwide Cyber Security Awareness Week (CSAW) Embedded System Challenge Competition 2017
- University of Delaware Research Foundation Strategic Initiative (UDRF-SI) Award 2015
- Best paper nomination in IFIP/IEEE International Conference on VLSI and System-on-Chip (VLSI-SoC) 2015
- National Science Foundation (NSF) CAREER Award 2013
- Best paper award in 16th IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2013
- University of Delaware Research Foundation (UDRF) Award 2011
- Best paper nomination in International Conference on Hardware/Software Co-Design and System Synthesis (CODES-ISSS) 2009
- UCSD Graduate Student Fellowship 2003
- Samsung Scholarship in Peking University, China 2002
- Dongshi Scholarship in Peking University, China 2001
- Guangcai Scholarship in Peking University, China 2000

Awards received by doctoral students under my supervision:

- Chen Liu (graduated in 2016)

- ✓ 2015-2016 University of Delaware Graduate Fellow Award
- ✓ 2014 Computer Systems and Networking Graduate Faculty Award
- ✓ 2013 Best paper and presentation award in *16th IEEE Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*

- Hoda Aghaeikhouzani (graduated in 2018)
  - ✓ 2017-2018 University of Delaware Doctoral Fellowship Award
  - ✓ 2016 University of Delaware ECE Research Day Outstanding Project Award
  - ✓ 2015 ECE Computer Systems and Networking Graduate Faculty Award
  - ✓ 2014 University of Delaware ECE Research Day Outstanding Project Award
- Yuan Xue (graduated in 2018)
  - ✓ 2017 Best paper nomination in *Design Automation Conference (DAC)*
  - ✓ 2015 University of Delaware ECE Research Day Outstanding Project Award
- Fateme Hosseini (4th year)
  - ✓ 2018 1st place in Worldwide Cyber Security Awareness Week (CSAW) Embedded System Challenge Competition
  - ✓ 2017 2nd place in Worldwide Cyber Security Awareness Week (CSAW) Embedded System Challenge Competition
- Patrick Cronin (3rd year)
  - ✓ 2018 1st place in Worldwide Cyber Security Awareness Week (CSAW) Embedded System Challenge Competition
  - ✓ 2018 University of Delaware ECE Research Day Outstanding Project Award
  - ✓ 2017 2nd place in Worldwide Cyber Security Awareness Week (CSAW) Embedded System Challenge Competition
  - ✓ 2017 University of Delaware ECE Research Day Outstanding Project Award
  - ✓ 2017 NSF GRFP Honorable Mention
  - ✓ 2016 NSF GRFP Honorable Mention
  - ✓ 2016 University of Delaware ECE Peter J. Warter Scholarship

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Research Grants:

Total cumulative funding (personal allocation, all as PI) $1.02M.

Awarded:

- **Principle Investigator:** CPS: Medium: Collaborative Research: Constantly on the Lookout: Low-Cost Sensor Enabled Explosive Detection to Protect High Density Environments
  National Science Foundation (NSF) $180,000 10/17 – 09/20
- **Principle Investigator:** SHF: Small: Collaborative:Multi-level Non-volatile FPGA Synthesis to Empower Efficient Self-adaptive System Implementations
  National Science Foundation (NSF) $266,000 09/15 – 08/19
- **Principle Investigator:** CAREER: Adaptively Boosting Resilience Efficiency in the Face of Frequent, Clustered, and Diverse Faults
  National Science Foundation (NSF) $481,500 06/13 – 05/19
- **Principle Investigator:** Building Trustworthy Cyber Physical Systems with Untrusted Devices
  University of Delaware Research Foundation (UDRF) $55,000 12/15 – 07/18

- **Principle Investigator:** Efficient Energy and Thermal Management through Application- and Architecture-Specific Optimizations
  University of Delaware Research Foundation (UDRF) $38,000 06/11 – 05/13

Publications:

Journal Publications:

[J20] Fanruo Meng, Yuan Xue, and **Chengmo Yang**, "Power- and Endurance-Aware Neural Network Training in NVM-based Platforms," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, 2018.

[J19] Patrick Cronin, Fateme Hosseini, and **Chengmo Yang**, "Building Fault Tolerant Assembly Lines with Untrusted Legacy Controllers," in IEEE Embedded Systems Letters *(**ESL**)*, 2018.

[J18] Jinshan Yue, Yongpan Liu, Zhe Yuan, Zhibo Wang, Qiuwei Guo, Jinyang Li, **Chengmo Yang**, Huazhong Yang, "A 3.77TOPS/W Convolutional Neural Network Processor with Priority-Driven Kernel Optimization," in *IEEE Transactions on Circuits and Systems II (**TCAS2**)*, 2018.

[J17] Chen Liu, Patrick Cronin, and **Chengmo Yang**, "Securing Cyber-Physical Systems from Hardware Trojan Collusion," in *ACM Transactions on Embedded Computing Systems (**TETC**)*, 2018.

[J16] Laura Rozo Duque, Aaron Myles Landwehr, Yan Zheng, **Chengmo Yang**, and Guang R. Gao, "Reliability-Aware Runtime Adaption through a Statically Generated Task Schedule," in *IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**)*, vol.26, no.1, pp. 11-22, 2018.

[J15] Chen Liu, Hoda Aghaeikhouzani, and **Chengmo Yang**, "ErasuCrypto: A low-overhead and Lifetime-friendly Data Destruction Scheme for Solid State Drives," in *Proceedings on Privacy Enhancing Technologies (**PoPETS**)*, pp. 132-148, 2017.

[J14] Hoda Aghaei Khouzani and **Chengmo Yang**, "A DWM-based Stack Architecture Implementation for Energy Harvesting Systems," in *ACM Transactions on Embedded Computing Systems (**TECS**)*, vol.15, no.5s, 2017.

[J13] Hoda Aghaei Khouzani and **Chengmo Yang**, "Segment and Conflict Aware Page Allocation and Migration in DRAM-PCM Hybrid Main Memory," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, vol.36, no.9, pp. 1458-1470, 2017.

[J12] Chen Pan, Mimi Xie, **Chengmo Yang**, Yiran Chen, and Jingtong Hu, "Exploiting Multiple Write Modes of Non-volatile Main Memory in Embedded Systems," in *ACM Transactions on Embedded Computing Systems (**TECS**)*, vol.16, no.4, 2017.

[J11] Yuan Xue and **Chengmo Yang**, "Path Reuse-aware Routing for Non-volatile Memory based FPGAs," in *Elsevier VLSI, the integration journal*, vol.58, pp. 505-517, 2017.

[J10] Yuanhui Ni, Zhiyao Gong, Weiwen Chen, **Chengmo Yang**, and Keni Qiu, "State-Transition-Aware Spilling Heuristic for MLC STT-RAM-Based Registers," in *VLSI Design Journal*, Hindawi, 2017.

[J9] Mengying Zhao, Yuan Xue, Jingtong Hu, **Chengmo Yang**, Tiantian Liu, Zhiping Jia, and Chun Jason Xue, "State Asymmetry Driven State Remapping in Phase Change Memory," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, vol.36, no.1, pp. 27-40, 2017.

[J8] Hoda Aghaeikhouzani, Yuan Xue, and **Chengmo Yang**, "Fully Exploiting PCM Write Capacity within Near Zero Cost through Segment-based Page Allocation," in *ACM Journal on Emerging Technologies in Computing Systems (**JETC**),* vol.12, no.4, May 2016.

[J7] Chen Liu, Jeyavijayan Rajendran, **Chengmo Yang**, and Ramesh Karri, "Shielding Heterogeneous MPSoCs from Untrustworthy 3PIPs through Security-Driven Task Scheduling," in *IEEE Transactions on Emerging Topics in Computing (**TETC**)*, vol.2, no.4, pp. 461-472, 2014.

[J6] Liang Shi, Jianghua Li, Qingan Li, Chun J. Xue, **Chengmo Yang**, and Xuehai Zhou, "A Unified Write Buffer Cache Management Scheme for Flash Memory," in *IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**),* vol. 22, no. 12, pp. 2779-2792, 2014.

[J5] **Chengmo Yang** and Alex Orailoglu, "Tackling Resource Variations through Adaptive Multicore Execution Frameworks," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**),* vol. 31, no. 1, pp. 132-145, January 2012.

[J4] **Chengmo Yang** and Alex Orailoglu, "Full Fault Resilience and Relaxed Synchronization Requirements at the Cache-Memory Interface," in *IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**)*, vol. 19, no. 11, pp. 1996-2009, November 2011.

[J3] Yuping Zhang, Chun J. Xue, **Chengmo Yang**, and Alex Orailoglu, "Migration-aware adaptive MPSoC static schedules with dynamic reconfigurability," in *Journal of Parallel and Distributed Computing (**JPDC**)*, vol. 71, no. 10, pp. 1400-1410, July 2011.

[J2] Wenjing Rao, **Chengmo Yang**, Ramesh Karri, and Alex Orailoglu, "Towards Future Systems with Nanoscale Devices: Overcoming the Reliability Challenge," in *IEEE Computer, special issue on Nanoscale Architectures*, vol. 44, no. 2, pp. 46-53, February 2011.

[J1] **Chengmo Yang**, Mingjing Chen, and Alex Orailoglu, "Minimizing On-chip Code Storage in Microcoded IPs while Delivering High Decompression Speed," in *Journal on Design Automation for Embedded Systems (**DAEM**)*, vol. 14, no. 3, pp. 265-284, July 2010.

Peer Reviewed Conference Publications:

[C60] Fateme Hosseini, Pouya Fotouhi, **Chengmo Yang**, and Guang R. Gao, "Comprehensive Evaluation of Program Reliability with ComFIDet: An Integrated Fault Injection and Detection Framework (Tool)," submitted to *International Conference on Dependable Systems and Networks (**DSN**)*, June 2019.

[C59] Shunzhuo Wang, Fei Wu, **Chengmo Yang**, Jiaona Zhou, Changsheng Xie, Jigang Wan, "WAS: Prolong the Lifetime of SSDs via A Wear Aware Superblock Management," submitted to *Design Automation Conference (**DAC**)*, June 2019.

[C58] Tao Liu, Wujie Wen, Lei Jiang, Yanzhi Wang, **Chengmo Yang**, and Gang Quan, "A Fault Tolerant Neural Network Architecture," submitted to *Design Automation Conference (**DAC**)*, June 2019.

[C57] Zeyu Chen and **Chengmo Yang**, "A Processing-In-Memory Implementation of SHA-3 Using a Voltage-Gated Spin Hall-Effect Driven MTJ-based Crossbar," submitted to *Great Lakes Symposium on VLSI (**GLSVLSI**)*, May 2019.

[C56] Hoda Aghaeikhouzani, Fateme Hosseini, and **Chengmo Yang**, "Cache Layout Exploration in Domain Wall Memory," submitted to *Great Lakes Symposium on VLSI (**GLSVLSI**)*, May 2019.

[C55] Yuan Xue and **Chengmo Yang,** "A Scalable and Process Variation-aware NVM FPGA Placement Algorithm," submitted to *Great Lakes Symposium on VLSI (**GLSVLSI**)*, May

2019.

[C54] Patrick Cronin and **Chengmo Yang**, "A Fetching Tale: Covert the Communication with the Hardware Prefetcher," submitted to *IEEE Symposium on Hardware Oriented Security and Trust* (***HOST***), May 2019.

[C53] Fateme Hosseini and **Chengmo Yang**, "Compiler-Directed and Architecture-Independent Mitigation of Read Disturbance Errors in STT-RAM," in *Design, Automation and Test in Europe (**DATE**)*, March 2019. Acceptance Rate: 25%.

[C52] Weihua Liu, Fei Wu, Meng Zhang, Yifei Wang, **Chengmo Yang**, Yifan Qiao, Jiguang Wan and Changsheng Xie, "EPS: Exploiting an Error Prechecking Scheme to Improve the Read Performance of SSD," submitted to *International Conference on Computer Design* (***ICCD***), 2018.

[C51] Hoda Aghaeikhouzani, Chen Liu, and **Chengmo Yang**, "Architecting Data Placement in SSDs for Efficient Secure Deletion Implementation," in *IEEE International Conference on Computer-Aided Design (**ICCAD**)*, November 2018.

[C50] Patrick Cronin, **Chengmo Yang**, and Yongpan Liu, "Reliability and Security in Non-Volatile Processors, Two Sides of the Same Coin," in *IEEE Computer Society Annual Symposium on VLSI* (**ISVLSI**), invited paper, July 2018.

[C49] Xinyi Zhang, Patterson Clay, Yongpan Liu, **Chengmo Yang**, Chun Jason Xue, and Jingtong Hu, "Low Overhead Online Checkpoint for Intermittently Powered Non-volatile FPGAs," in *IEEE Computer Society Annual Symposium on VLSI* (**ISVLSI**), July 2018.

[C48] Patrick Cronin, **Chengmo Yang**, and Yongpan Liu, "A Collaborative Defense against Wearout Attacks in Non-Volatile Processors," in *Design Automation Conference (**DAC**)*, June 2018.

[C47] Fei Wu, Jiaona Zhou, Shunzhuo Wang, Yajuan Du, **Chengmo Yang**, and Changsheng Xie, "FastGC: Accelerate Garbage Collection via an Efficient Copyback-based Data Migration in SSDs," in *Design Automation Conference (**DAC**)*, June 2018.

[C46] Qingwei Guo, Yoshinori Miyamae, Zhongjun Wang, Koji Taniuchi, Guijin Wang, **Chengmo Yang**, Huazhong Yang, and Yongpan Liu, "Senvis-Net: Learning from Imbalanced Machinery Data by Transferring Visual Element Detectors," in *2nd International Conference on Advanced Manufacturing and Materials (*ICAMM 2018*)*, June 2018.

[C45] Patrick Cronin and **Chengmo Yang**, "Lowering the Barrier to Online Malware Detection Through Low Frequency Sampling of HPCs," in *IEEE Symposium on Hardware Oriented Security and Trust* (***HOST***), pp. 177-180, May 2018.

[C44] Hongbin Zhang, Chao Zhang, Qingda Hu, Chengmo Yang, Jiwu Shu, "Performance Analysis on Structure of Racetrack Memory," in *23rd Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 3607-374, January 2018.

[C43] Meng Zhang, Fei Wu, Yajuan Du, **Chengmo Yang** Changsheng Xie and Jiguang Wan, "CooECC: A Cooperative Error Correction Scheme to Reduce LDPC Decoding Latency in NAND Flash," in 35th *International Conference on Computer Design* (***ICCD***), pp. 657-664, November 2017. Acceptance Rate: 29%.

[C42] Yuan Xue, Abraham Mcllvaine, **Chengmo Yang,** "Power-aware and Cost-efficient State Encoding in Non-volatile Memory based FPGAs," in *International Conference on VLSI and System-on-Chip (**VLSI-SoC**)*, October 2017. Acceptance Rate: 29%.

[C41] Patrick Cronin, **Chengmo Yang**, Dongqin Zhou, Keni Qui, Xin Shi and Yongpan Liu, "'The Dangers of Sleeping', an Exploration of Security in Non-Volatile Processors," in *IEEE Asian Hardware Oriented Security and Trust Symposium* (***AsianHOST***), October 2017.

[C40] Qiao Li, Liang Shi, Yejia Di, Yajuan Du, Chun Jason Xue, **Chengmo Yang**, Qingfeng Zhuge and Edwin Sha**,** "Improving Read Performance Via Selective Vpass Reduction on High Density 3D NAND Flash Memory," in *6th IEEE Non-Volatile Memory Systems and Applications Symposium (**NVMSA**)*, pp. 1-4, August 2017.

[C39] Yuan Xue, **Chengmo Yang**, and Jingtong Hu, "Age-aware Logic and Memory Co-Placement for RRAM-based FPGAs," in *Design Automation Conference (**DAC**)*, June 2017. Acceptance Rate: 22%. **(Best Paper Nomination)**

[C38] Fateme Hosseini, Pouya Fotouhi, **Chengmo Yang**, and Guang R. Gao, "Leveraging Compiler Optimizations to Reduce Runtime Fault Recovery Overhead," in *Design Automation Conference (**DAC**)*, June 2017. Acceptance Rate: 22%.

[C37] Hoda Aghaei Khouzani, Pouya Fotouhi, **Chengmo Yang**, and Guang R. Gao, "Leveraging Access Port Positions to Accelerate Page Table Walk in DWM-based Main Memory," in *Design, Automation and Test in Europe (**DATE**)*, pp. 1450-1455, March 2017. Acceptance Rate: 23%.

[C36] Hoda Aghaeikhouzani and **Chengmo Yang**, "Exploiting Remap-on-write in Solid State Drives towards an Efficient Multi-version Checkpointing Scheme," in *46th International Conference on Dependable Systems and Networks (**DSN**)*, pp. 37-48, June 2016. Acceptance Rate: 22%.

[C35] Yuan Xue, Patrick Cronin, **Chengmo Yang**, and Jingtong Hu, "Routing Path Reuse Maximization for Efficient NV-FPGA Reconfiguration," in *21st Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 360-365, January 2016, Acceptance Rate: 33%.

[C34] Chen Liu, Patrick Cronin, and **Chengmo Yang**, "A Mutual Auditing Framework to Protect IoT against Hardware Trojans," in *21st Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 69-74, January 2016. Acceptance Rate: 33%.

[C33] Yuan Xue, Patrick Cronin, **Chengmo Yang**, and Jingtong Hu, "Non-volatile Memories in FPGAs: Exploiting Logic Similarity to Accelerate Reconfiguration and Increase Programming Cycles," in *International Conference on VLSI and System-on-Chip (**VLSI-SoC**)*, pp. 92-97, October 2015. Acceptance Rate: 36%.

[C32] **Chengmo Yang** and Maria Ruiz Varela**,** "Qualifying Non-Volatile Register Files for Embedded Systems through Compiler-directed Write Reduction and Balancing," in *International Conference on VLSI and System-on-Chip (**VLSI-SoC**)*, pp. 86-91, October 2015. Acceptance Rate: 36%. **(best paper nomination)**

[C31] Chen Pan, Mimi Xie, **Chengmo Yang**, Zili Shao, and Jingtong Hu, "Nonvolatile Main Memory Aware Garbage Collection in High-Level Language Virtual Machine," in *International Conference on Embedded Software (**EMSOFT**)*, pp. 197-206, October 2015. Acceptance Rate: 25%.

[C30] Yuan Xue, Patrick Cronin, **Chengmo Yang**, and Jingtong Hu, "Fine-tuning CLB Placement to Speed up Reconfiguration and Improve Endurance of NVM-based FPGAs," in *25th International Conference on Field-programmable Logic and Applications* (***FPL***), pp. 1-8, September 2015. Acceptance Rate: 22%.

[C29] Chen Liu and **Chengmo Yang**, "Secure and Durable (SEDURA): An Integrated Encryption and Wear-leveling Framework for PCM-based Main Memory," in *16th Conference on Languages, Compilers, and Tools for Embedded Systems (**LCTES**)*, June 2015. Acceptance Rate: 26%.

[C28] Laura Rozo Duque, Jose Monsalve, and **Chengmo Yang**, "Improving MPSoC Reliability

through Adapting Runtime Application Schedule based on Time-Correlated Fault Behavior," in *Design, Automation and Test in Europe (**DATE**)*, pp. 818-823, March 2015. Acceptance Rate: 22%.

[C27] Laura Rozo Duque and **Chengmo Yang**, "Guiding Fault-driven Runtime Adaption in Multicore Systems through a Pre-optimized Reliability-aware Task Schedule," in *20th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 612-617, January 2015. Acceptance Rate: 34%.

[C26] Hoda Aghaeikhouzani, **Chengmo Yang**, and Jingtong Hu, "Improving Performance and Lifetime of DRAM-PCM Hybrid Main Memory through a Proactive Page Allocation Strategy," in *20th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 508-513, January 2015. Acceptance Rate: 34%.

[C25] Mengying Zhao, Yuan Xue, **Chengmo Yang**, and Chun J. Xue, "Minimizing Write Energy for MLC Phase Change Memory through Near-zero-cost State Remapping," in *20th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 502-507, January 2015. Acceptance Rate: 34%.

[C24] Mimi Xie, Chen Pan, Jingtong Hu, **Chengmo Yang**, and Yiran Chen, "Checkpoint-Aware Instruction Scheduling for Nonvolatile Processor with Multiple Functional Units," in *20th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 316-321, January 2015. Acceptance Rate: 34%.

[C23] Chen Liu and **Chengmo Yang**, "Improving Multilevel PCM Reliability through Age-aware Reading and Writing Strategies," in *32nd International Conference on Computer Design* (***ICCD***), pp. 264-269, October 2014. Acceptance Rate: 31%.

[C22] Mengying Zhao, Liang Shi, **Chengmo Yang**, and Chun J. Xue, "Leveling to the Last Mile: Near-zero-cost Bit Level Wear Leveling for PCM based Main Memory," in *32nd International Conference on Computer Design* (***ICCD***), pp. 16-21, October 2014. Acceptance Rate: 31%.

[C21] Chen Liu, **Chengmo Yang,** and Yuanqi Shen, "Leveraging Microarchitectural Side Channel Information to Enhance Control Flow Integrity," in *International Conference on Hardware/ Software Codesign and System Synthesis (**CODES-ISSS**)*, pp. 1-9, October 2014. Acceptance Rate: 25%.

[C20] Chen Pan, Mimi Xie, Jingtong Hu, Yiran Chen, and **Chengmo Yang**, "3M-PCM: Exploiting Multiple Write Modes MLC Phase Change Main Memory in Embedded Systems," in *International Conference on Hardware/Software Codesign and System Synthesis (**CODES-ISSS**)*, pp. 1-10, October 2014. Acceptance Rate: 25%.

[C19] Hoda Aghaeikhouzani, Yuan Xue, **Chengmo Yang**, and Archana Pandurangi, "Prolonging PCM Lifetime through Energy-efficient, Segment-aware, and Wear-resistant Page Allocation," in *International Symposium on Low Power Electronics and Design* (***ISLPED***), pp. 327-330, August 2014. Acceptance Rate: 34%.

[C18] Chen Liu and **Chengmo Yang**, "Exploiting Heterogeneity in MPSoCs to Prevent Trojan Propagation across Malicious 3PIPs," in *24th Great Lakes Symposium on VLSI (**GLSVLSI**)*, pp. 335-340, May 2014. Acceptance Rate: 27%.

[C17] Hao Chen and **Chengmo Yang**, "Fault Detection and Recovery Efficiency Co-optimization through Compile-time Analysis and Runtime Adaptation," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (**CASES**)*, pp. 1-10, October 2013. Acceptance Rate: 30%.

[C16] Chen Liu, Jeyavijayan Rajendran, **Chengmo Yang**, and Ramesh Karri, "Shielding Heterogeneous MPSoCs from Untrustworthy 3PIPs through Security-Driven Task Scheduling," in *16th International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT**)*, pp. 101-106, October, 2013. **(best student paper and presentation award)**

[C15] Hao Chen and **Chengmo Yang**, "Boosting Efficiency of Fault Detection and Recovery through Application-Specific Comparison and Checkpointing," in *14th Conference on Languages, Compilers, and Tools for Embedded Systems (**LCTES**)*, pp. 13-20, June, 2013. Acceptance Rate: 26%.

[C14] Tianzheng Wang, Duo Liu, Zili Shao, and **Chengmo Yang**, "Write-Activity-Aware Page Table Management for PCM-based Embedded System," in *17th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, pp. 317-322, January 2012. Acceptance Rate: 34%.

[C13] Liang Shi, Jianghua Li, Chun J. Xue, **Chengmo Yang**, and Xuehai Zhou, "ExLRU: A Unified Write Buffer Cache Management for Flash Memory," in *International Conference on Embedded Software (**EMSOFT**)*, pp. 339-348, October 2011. Acceptance Rate: 24%.

[C12] Jianghua Li, Liang Shi, Chun J. Xue, **Chengmo Yang**, and Yinlong Xu, "Exploiting Set-Level Write Non-Uniformity for Energy-Efficient NVM-Based Hybrid Cache," in *9th Symposium on Embedded Systems for Real-Time Multimedia (**ESTIMedia**)*, pp. 19-28, October 2011.

[C11] **Chengmo Yang** and Alex Orailoglu, "Frugal Fixed Silicon but Flexible Topologies for Multicore Platforms in Support of Resource Variation-Driven Adaptivity," in *Design, Automation and Test in Europe (**DATE**)*, pp. 1-6, March 2011.

[C10] **Chengmo Yang** and Alex Orailoglu, "Fully Adaptive Multicore Architectures through Statically-directed Dynamic Execution Reconfigurations," in *International Conference on VLSI and System-on-Chip (**VLSI-SoC**)*, pp. 396-401, September 2010.

[C9] **Chengmo Yang**, Chun J. Xue, and Alex Orailoglu, "Fine-grained Adaptive CMP Cache Sharing through Access History Exploitation," in *International Conference on VLSI and System-on-Chip (**VLSI-SoC**)*, pp. 420-425, September 2010.

[C8] **Chengmo Yang**, MingjingChen, and Alex Orailoglu, "Squashing Microcode Stores to Size in Embedded Systems while Delivering Rapid Microcode Accesses," in *International Conference on Hardware/Software Codesign and System Synthesis (**CODES-ISSS**)*, pp. 249-256, October 2009. **(best paper nomination)**

[C7] **Chengmo Yang** and Alex Orailoglu, "Processor Reliability Enhancement through Compiler-Directed Register File Peak Temperature Reduction," in *39th International Conference on Dependable Systems and Networks (**DSN**)*, pp. 468-477, June 2009.

[C6] **Chengmo Yang** and Alex Orailoglu, "Towards No-cost Adaptive MPSoC Static Schedules through Exploitation of Logical-to-physical Core Mapping Latitude," in *Design, Automation and Test in Europe (**DATE**)*, pp. 63-68, April 2009.

[C5] **Chengmo Yang** and Alex Orailoglu, "A Light-weight Cache-based Fault Detection and Checkpointing Scheme for MPSoCs Enabling Relaxed Execution Synchronization," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (**CASES**),* pp. 11-20, October 2008.

[C4] **Chengmo Yang** and Alex Orailoglu, "Predictable Execution Adaptivity through Embedding Dynamic Reconfigurability into Static MPSoC Schedules," in *International Conference on Hardware/Software Codesign and System Synthesis (**CODES-ISSS**)*, pp. 15-20, October 2007.

[C3] **Chengmo Yang** and Alex Orailoglu, "Light-weight Synchronization for Inter-processor Communication Acceleration on Embedded MPSoCs," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (**CASES**),* pp. 150-154, October 2007.

[C2] **Chengmo Yang** and Alex Orailoglu, "Power-efficient Branch Prediction through Early Identification of Branch Addresses," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (**CASES**),* pp. 169-178, October 2006.

[C1] **Chengmo Yang** and Alex Orailoglu, "Power-efficient Instruction Delivery through Trace Reuse," in *15th International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, pp. 192-201, September 2006.

Workshop Papers/Posters:

[W3] **Chengmo Yang** and Maria Ruiz Varela**,** "Qualifying Non-Volatile Register Files for Embedded Systems through Compiler-directed Write Reduction and Balancing," in *Memory Architecture and Organization Workshop (**MeAOW**)*, October 2014.

[W2] Laura Rozo Duque, Jose Monsalve and **Chengmo Yang,** "Adapting Fault Resilience Granularity to Overcome Varying Failure Rates in CPS," in *NSF Young Professional Workshop on Exploring New Frontiers in Cyber-Physical Systems*, March 2014.

[W1] **Chengmo Yang** and Alex Orailoglu, "Accelerating Coupled Applications through Register Level Communication between Processing Elements," in *4th Workshop on Application Specific Processors (**WASP**)*, pp. 51-59, September 2005.

Invited Talks:

[T27] "You Just Have to Know Where to Look: Leveraging Invisible Processor Features for Attack and Defense," in Intel, November 2018.

[T26] "Towards Secure, Reliable, and Non-volatile Embedded Systems Design," in Department of Electrical and Computer Engineering, University of California, Riverside, November 2018.

[T25] "Building Trustworthy System with Untrusted Components: Countermeasures against Hardware Trojans Collusion," in Department of Computer Science and Engineering, University of California, San Diego, November 2018.

[T24] "Cost-effective Secure Deletion in Solid State Drives" in School of Computer Science and Technology, Huazhong University of Science and Technology, China, August 2018.

[T23] "Domain Wall Memory: is it the technology to replace CMOS in future embedded and IoT devices?" in College of Computer Science, Chongqing University, China, July 2018.

[T22] "NVM-friendly FPGA Synthesis," in Department of Electrical and Computer Engineering, University of Pittsburgh, March 2018.

[T21] "NVM-friendly FPGA Synthesis," in Department of Electrical Engineering, Zhejiang University, China, December 2017.

[T20] "NVM-friendly FPGA Synthesis," in School of Computer Science and Technology, Shandong University, China, December 2017.

[T19] "NVM-friendly FPGA Synthesis," in Department of Computer Science and Engineering, Chinese University of Hong Kong, December 2017.

[T18] "Building Trustworthy System with Untrusted Components: Countermeasures against Hardware Trojans Collusion," in Department of Electrical and Computer Engineering, Hong Kong University of Science and Technology, December 2017.

[T17] "Building Trustworthy System with Untrusted Components: Countermeasures against Hardware Trojans Collusion," in New York University Abu Dhabi, October 2017.

[T16] "Towards a Scalable and Write-free Multi-version Checkpointing Scheme in Solid State Drives," in School of Computer Science and Technology, Huazhong University of Science and Technology, China, April 2017.

[T15] "Runtime Solutions to Apply Non-volatile Memories in Future Computer Systems," in College of Information Engineering, Capital Normal University, China, April 2017.

[T14] "Building Trustworthy System with Untrusted Components: Countermeasures against Hardware Trojans Collusion," in School of Computer Science and Technology, Anhui University, March 2017.

[T13] "Building Trustworthy System with Untrusted Components: Countermeasures against Hardware Trojans Collusion," in Department of Electrical and Computer Engineering, Drexel University, October 2016.

[T12] "NVM-friendly Placement and Routing in FPGAs," in Department of Computer Science, Zhejiang University, China, January 2016.

[T11] "NVM-friendly Placement and Routing in FPGAs," in School of Computer Science and Technology, Shandong University, China, January 2016.

[T10] "Boosting Efficiency of Fault Detection and Recovery through Application-Specific Comparison and Checkpointing," in *Workshop on Compiler-assisted System-on-chip Assembly (**CASA**)*, New Delhi, India, October 2014.

[T9] "Qualifying Non-Volatile Register Files for Embedded Systems through Compiler-directed Write Reduction and Balancing," in *Memory Architecture and Organization Workshop (**MeAOW**)*, New Delhi, October 2014.

[T8] "The Need for More Comprehensive Benchmarks to Model Heterogeneous MPSoCs," in *Workshop on Benchmarking Embedded Systems (**BES**)*, Montreal, Canada, September 2013.

[T7] "Towards Efficient Fault Tolerance in Future Computer Systems," in Department of Computer Science and Engineering, Shanghai Jiaotong University, China, May 2013.

[T6] "Towards Efficient Fault Tolerance in Future Computer Systems," in Department of Computer Science, Zhejiang University, China, May 2013.

[T5] "Towards Efficient Fault Tolerance in Future Computer Systems," in College of Computer Science, Chongqing University, China, May 2013.

[T4] "Tackling Computation Uncertainty through Fine-grained and Predictable Execution Adaptivity in Multi/Many Core Systems", in Exascale Computer Research Lab, University of Versailles Saint Quentin, Versailles, France, March 2011.

[T3] "Tackling Computation Uncertainty through Fine-grained and Predictable Execution Adaptivity in Multi/Many Core Systems," in Department of Software Engineering, Tsinghua University, China, January 2011.

[T2] "Tackling Computation Uncertainty through Fine-grained and Predictable Execution Adaptivity in Multi/Many Core Systems," in Department of Computing, Hong Kong Polytechnic University, Hong Kong, December 2010.

[T1] "Tackling Computation Uncertainty through Fine-grained and Predictable Execution Adaptivity in Multi/Many Core Systems," in Department of Computer Science, City University of Hong Kong, Hong Kong, December 2010.

Courses Taught:

- CPEG 202: "Introduction to Digital Systems" Spring 2012 Enrollment 88

  Description: Analysis and design of logic circuits. Topics include: Boolean algebra and its application to digital circuits, simplification of Boolean functions, design of combinational circuits at gate level and at component level. Analysis and design of synchronous and asynchronous sequential state machines.

- CPEG 222: "Microprocessor Systems" Spring 2016 Enrollment 101
  Spring 2015 Enrollment 65
  Spring 2014 Enrollment 48
  Spring 2013 Enrollment 44

  Description: Introduction to microprocessors as embedded devices. Emphasizes input/output devices, interrupts, real-time operations, high-level code debugging and interfacing to various types of sensors and actuators. Projects that address various embedded applications are a major part of the course. **Final project is organized as a departmental annual robot competition.**

- CPEG 422/622: "Embedded Systems Design" Spring 2018 Enrollment 7
  Spring 2019 Enrollment 11

  Description: Provides an introduction to hardware/software co-design of embedded systems. Topics include, but are not limited to, VHDL, IP cores and customization, Memory, bus, and IO devices, Matrix multiplication, DSP, Cybersecurity, etc.

- ELEG/CPEG 652: "Principles of Parallel Architectures" Fall 2016 Enrollment 9
  Fall 2015 Enrollment 11
  Fall 2013 Enrollment 11
  Fall 2011 Enrollment 14

  Description: Provides an introduction to the principles of parallel computer architectures. Topics include, but are not limited to, introduction-level, thread-level, and processor-level parallelism, pipelining, branch prediction, memory hierarchy, coherency and consistency, runtime and compile-time optimizations, etc.

- ELEG 662: "Digital Systems Seminar" Spring 2018 Enrollment 20
  Spring 2016 Enrollment 40
  Fall 2013 Enrollment 23

  Description: A weekly lecture and discussion on specialized topics in digital systems. It introduces graduate students to different research topics in the computer engineering area. Many internal and external speakers are invited.

- CPEG 853: "Reliable Computer Systems" Fall 2018 Enrollment 5
  Fall 2016 Enrollment 9
  Fall 2014 Enrollment 7
  CPEG 867: "Reliable Computer Systems" Fall 2012 Enrollment 7
  CPEG 467/667: "Reliable Computer Systems" Spring 2011 Enrollment 3

Description: Introduction to reliability challenges in computer systems, including permanent, transient, and intermittent faults. Various types of redundancy for fault tolerant computing are studied. Hardware/software approaches for reliability enhancement in various computer systems are examined, emphasizing tradeoffs involving performance, power, and reliability.

Professional Activities:

Editorial Board:

- **[TCAD]** IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems
  Associate Editor
- **[TODAES]** ACM Transactions on Design Automation of Electronic Systems
  Associate Editor

Conference Organizations:

- **[ESWeek 2019]** Embedded Systems Week
  Publication Chair
- **[HOST 2019]** IEEE Symposium on Hardware Oriented Security and Trust
  Video & Audio Chair
- **[AsianHOST 2018]** Asian Hardware Oriented Security and Trust Symposium
  Panel Chair
- **[ISVLSI 2018-2019]** IEEE Computer Society Annual Symposium on VLSI
  Technical Program Track Chair – "System and Security"
- **[SLIP 2018]** ACM/IEEE System Level Interconnect Prediction Workshop
  Technical Program Co-Chair
- **[ICCD 2016-2017]** IEEE International Conference on Computer Design
  Special Session and Tutorial Chair

Technical Program Committee Member:

- **[CODES-ISSS 2011, 2017-2019**] Conference on Hardware/Software Co-Design and System Synthesis
- **[DATE 2018-2019]** Design, Automation and Test in Europe
- **[GLSVLSI 2018-2019]** ACM Great Lakes Symposium on VLSI
- **[HOST 2018-2019]** IEEE Symposium on Hardware Oriented Security and Trust
- **[ICCD 2014-2018]** IEEE International Conference on Computer Design
- **[ICCAD 2018]** IEEE International Conference on Computer-Aided Design
- **[ICESS 2018]** IEEE International Conference on Embedded Software Systems
- **[IS-VLSI 2014-2019]** IEEE Computer Society Annual Symposium on VLSI
- **[LCTES 2014-2019]** Conference on Languages, Compilers, and Tools for Embedded Systems
- **[VLSI-SoC 2013,2018]** International Conference on VLSI and System-on-Chip
- **[ASP-DAC 2015-2017, 2019]** Asia and South Pacific Design Automation Conference
- **[DAC 2019]** Design Automation Conference
- **[DSC 2017]** IEEE Conference on Dependable and Secure Computing
- **[NVMSA 2017]** IEEE Non-Volatile Memory Systems and Applications Symposium
- **[RTSS 2016]** IEEE Real-Time Systems Symposium

- **[BDPSS 2016]** Workshop on Big Data Programming and System Software
- **[LPDC 2016]** Workshop on Low-Power Dependable Computing
- **[MeAOW 2013–2014]** Workshop on Memory Architecture and Organization
- **[NPC 2013–2014]** International Conference on Network and Parallel Computing
- **[DFR 2012]** Workshop on Design for Reliability
- **[EUC 2011]** International Conference on Embedded and Ubiquitous Computing

Technical Reviewer:

- ACM: Journal on Emerging Technologies in Computing Systems (JETC)
- ACM: Transactions on Architecture and Code Optimization (TACO)
- ACM: Transactions on Embedded Computing Systems (TECS)
- ACM: Transactions on Design Automation of Electronic Systems (TODAES)
- Elsevier: Journal of Systems Architecture: Embedded Software Design (JSA)
- IEEE: Embedded Systems Letters (ESL)
- IEEE: Proceedings of the IEEE
- IEEE: Transactions on Computers (TC)
- IEEE: Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE: Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE: Transactions on Storage (TOS)
- Inderscience Publishers: International Journal of Embedded Systems (IJES)
- Springer: International Journal of Parallel Programming (IJPP)
- Springer: Journal of Signal Processing Systems
- Springer: Journal of Design Automation for Embedded Systems (DAEM)
- IEEE Design Automation Conference (DAC)
- Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
- Conference on Parallel Architecture and Compilation Techniques (PACT)
- Supercomputing Conference (SC)