Applied Surface Science 175–176 (2001) 505–511

applied surface science

www.elsevier.nl/locate/apsusc

The electrical characteristics of silicon carbide alloyed with germanium

G. Katulka[a,*], K. Roe[a], J. Kolodzey[a], G. Eldridge[b], R.C. Clarke[b], C.P. Swann[c], R.G. Wilson[d]

[a]*Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716, USA*
[b]*Electronic Sensors and Systems Division, Northrop Grumman, Linthicum, MD 21090, USA*
[c]*Bartol Research Institute, University of Delaware, Newark, DE 19716, USA*
[d]*Stevenson Ranch, CA 91381, USA*

Accepted 3 November 2000

Abstract

As an electronic material for high power, high voltage applications, silicon carbide (SiC) would be more versatile if suitable heterojunction partners were available. Using ion implantation, we have formed alloys of SiC with a few atomic percent of germanium (Ge). The Ge was implanted at 346 keV and a dose of 1.67×10^{16} cm^{-2} into a p-type 4H SiC wafer at room temperature, and followed by subsequent annealing up to 1700°C. Through X-ray diffraction (XRD) measurements it was determined that the Ge implanted SiC had a larger lattice constant which implies that some of the Ge is substitutional. The X-ray measurements indicated that a secondary peak attributable to substitutional Ge increases in intensity and shifted toward a lower Bragg angle as the implanted Ge dose was increased. SiC/SiC:Ge heterojunction devices were formed using titanium/gold (Ti/Au) as electrical contacts. Current–voltage (*I–V*) and capacitance measurements confirmed a reduction of the forward voltage drop and built-in voltage in SiC:Ge, compared to similar SiC devices without Ge. Other p-type substrates implanted with Ge that used chromium/nickel (Cr/Ni) metalization as electrical contacts were shown to have a significantly lower contact resistance compared to SiC. These results indicate that the SiC/SiC:Ge material system may be promising for SiC heterojunction device applications.

Keywords: SiC; Ge; Implantation; SiC:Ge; Alloys; *I–V* characteristics

1. Sample preparation

The goal of this study was to determine the effects of Ge on the properties of p- and n-type silicon carbide (SiC) for use in SiC/SiC:Ge heterostructure device applications. The measurement techniques included Rutherford backscattering spectrometry (RBS), X-ray diffraction (XRD), current–voltage (*I–V*), and capacitance–voltage (*C–V*). The SiC:Ge films were created by ion implantation into a p-type 4H SiC wafer from Cree Research doped p-type to 5×10^{16} cm^{-3}. The wafer was at room temperature during the ion implantation process. Approximately half of the wafer was implanted with nitrogen (N). The N implantation was performed in a series of four steps to achieve a uniform N profile in the wafer. The final N implant was from a 124 keV ion beam source with a dose of

* Corresponding author. Tel.: +1-302-831-8959; fax: +1-302-831-4316.
E-mail address: katulka@ee.udel.edu (G. Katulka).

0169-4332/01/$ – see front matter
PII: S0169-4332(01)00111-8

Table 1
SRIM calculations and SIMS results for Ge and N ion implantation into p-type, 4H SiC wafer for SiC/SiC:Ge diode study[a]

Implanted ion	Ion beam energy (KeV)	Dopant concentration (atoms/cm^3)	Calculated projected range (Å)	Calculated longitudinal straggle (Å)	Projected range from SIMS (Å)
Ge	346	8×10^{20}	1440	364	1500
N	124	1×10^{20}	1942	406	1980

[a] All implantation was performed at room temperature and the wafer implantation was performed in two steps. Approximately one-half of the wafer was implanted with Ge ions, then the wafer was rotated by 90° and another half was implanted with N ions.

9.0×10^{14} cm^{-2}, which gave a highly doped n-type region having a peak concentration of 1×10^{20} cm^{-3}. After rotating the wafer by 90°, it was implanted with Ge to approximately 8×10^{20} cm^{-3} from a 346 keV ion beam with a dose of 1.67×10^{16} cm^{-2}. This resulted in a wafer of quadrants with surface layers of SiC, with and without Ge and N. The projected ion range and longitudinal straggle values calculated with the SRIM program for the implanted ions are provided in Table 1 [1]. The implantation depths were confirmed with secondary ion mass spectroscopy (SIMS), which agreed well with the SRIM calculations and indicated similar depths for the Ge and N implants. After implantation, the substrate was annealed in steps up to a maximum temperature of 1700°C for 20 min.

2. Experimental results

The RBS data was obtained with a 2 MeV He$^+$ ion accelerator, for both the SiC and the SiC:Ge regions of the substrate. The data was compared to theoretical calculations using the Rutherford universal manipulation program (RUMP) [2]. The RBS data in Fig. 1 showed evidence of the underlying SiC substrate, the SiC:Ge surface layer, and a thin region of metalization on the surface from the electrical contacts. RUMP simulations yielded a SiC:Ge layer thickness of 2700 Å with a peak Ge concentration of 1.6%. This amount of Ge was also obtained in previous studies of SiC:Ge [3].

XRD was used to characterize the SiC:Ge crystalline structure including the lattice spacing relative to that of the SiC substrate. Measurements were performed with a Philips MRD diffractometer utilizing the Cu Kα_1 wavelength (1.54056 Å) in the symmetrical Bragg configuration. The results of the XRD measurements for the SiC substrate compared to that of the SiC:Ge region are given in Fig. 2. The XRD data for the 4H SiC substrate exhibits a sharp peak at 35.5° which corresponds to the (0004) plane of 4H SiC. The Ge implanted SiC region has an additional shoulder of lower intensity centered around 35.2°, which corresponds to a layer with a larger lattice constant that we attribute to substitutional Ge. From Vegard's law we predict 2.3% substitutional Ge in this layer.

Additional p-type 4H SiC samples were implanted with varying amounts of Ge to determine the effects of implanted Ge on crystallographic properties. XRD measurements were used to characterize these samples as well. The three curves in Fig. 3 show the X-ray data for samples with Ge doses of, 1×10^{15} cm^{-2} (low dose), 2×10^{16} cm^{-2} (medium dose), and 8×10^{16} cm^{-2} (high dose). Substitutional incorporation of Ge into the SiC lattice would result in a SiC:Ge

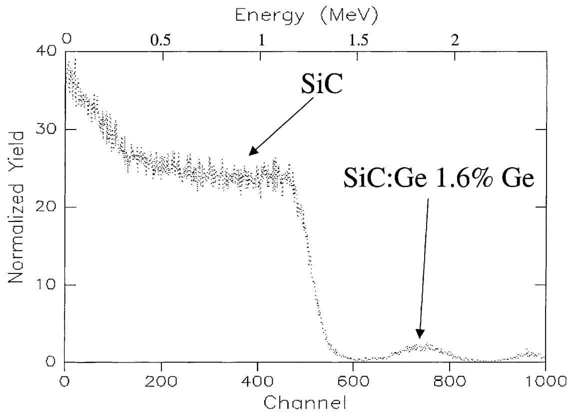

Fig. 1. RBS data from the SiC:Ge layer showing evidence of C, Si, and Ge profiles. The data was taken with a 2 MeV He$^+$ RBS system. The SiC RBS profile is evident below 1.2 MeV where the He$^+$ ions are scattered from Si atoms. C atoms in the SiC cause the increased scattering below 0.5 MeV. The Ge profile is seen at 1.8 MeV and a thin layer of heavy metal atoms causes the small peak at 2.4 MeV.

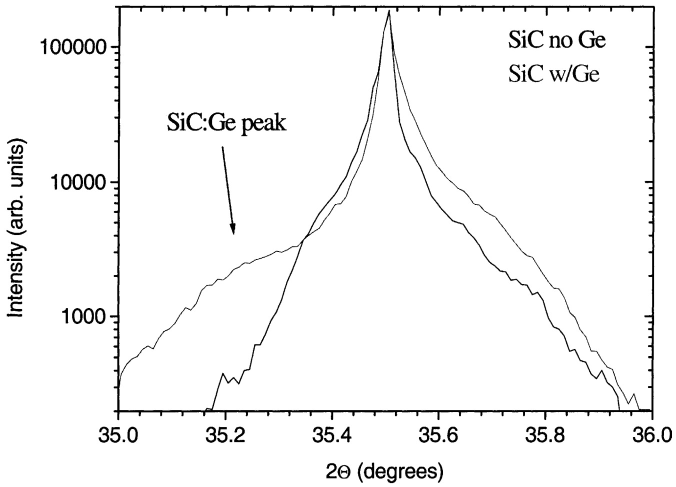

Fig. 2. X-ray diffraction data from SiC and Ge implanted SiC substrates. The data from the SiC:Ge sample is observed to have a Bragg reflection peak centered near 35.2°, while the (0004) plane of the SiC substrate is evident near 35.5°. X-ray data is taken with a Phillips MRD Diffractometer utilizing the Cu Kα_1 wavelength.

layer having a larger lattice constant due to larger atomic size of Ge. Such an effect would manifest itself as a secondary peak at a lower Bragg angle in the XRD measurement. The X-ray data of Fig. 3., shows how secondary peaks below 35.5° increased in height and shifted lower in Bragg angle as the implanted Ge dose was increased. The low and medium dose samples of Fig. 3 show relatively low intensity secondary peaks below the 4H SiC peak at 35.5°. For the high dose sample, however, a larger intensity secondary peak centered around 35.2° is observed. Based upon Vegard's law, this secondary peak at 35.2° corresponds

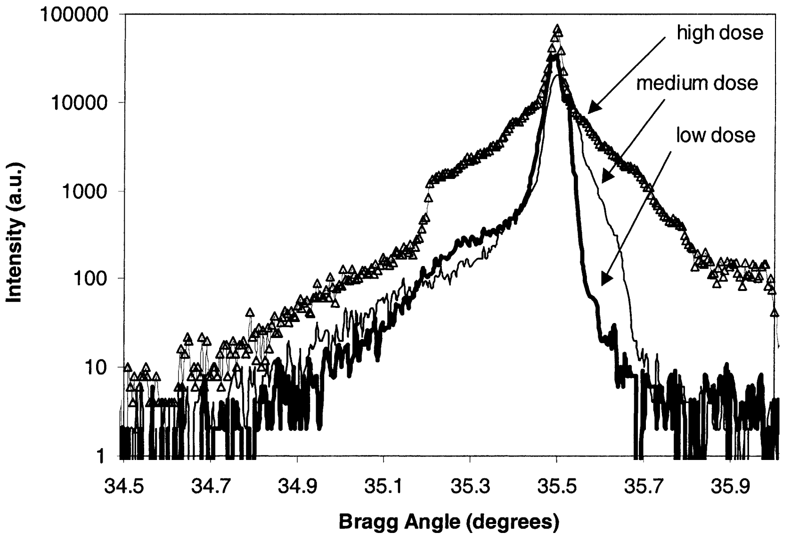

Fig. 3. X-ray diffraction data of three samples of SiC with varying amounts of Ge. The solid (thick) curve is for the low Ge dose implanted SiC sample (1×10^{15} cm^{-2}). The solid (thin) curve is for the medium Ge dose implanted SiC sample (2×10^{16} cm^{-2}), and the thin solid line with tick marks represents the high Ge dose sample (8×10^{16} cm^{-2}). All X-ray data was taken for the samples after implantation of Ge ions and an 800°C 1 min RTA anneal.

to approximately 2.3% substitutional Ge in the 4H SiC lattice. SRIM calculations predict an average Ge concentration of 3.46%, thus, 66.5% of the implanted Ge is considered substitutional. The X-ray intensity for Bragg angles slightly greater than the 4H SiC peak at 35.5° increased monotonically with the Ge implantation dose. This high angle shoulder, however, is attributed to lattice damage as a result of the Ge implantation process.

3. Electrical characteristics of SiC/SiC:Ge

Metal contacts were formed on the SiC/SiC:Ge wafer by the e-beam evaporation of Ti/Au directly onto the front and backside with an evaporation chamber pressure of approximately 1×10^{-7} Torr. Devices were formed with circular top contacts (137.5 μm diameter) and with a large area electrical contact on the backside of the wafer. The contacts were subsequently annealed in a rapid thermal annealer (RTA) to 800°C for 1 min in forming gas. Linear Ohmic contact behavior was confirmed by current–voltage measurements. The current–voltage (*I–V*) measurements were performed using a Hewlett–Packard 4156B parameter analyzer, and the lowest contact resistance achieved for the devices was approximately 1.75×10^{-1} ohm cm^2 for the SiC:Ge region of the wafer.

I–V data of the p–n junctions were taken before and after contact annealing. Fig. 4 shows the *I–V* data of devices located in the four regions of the wafer before contact anneals. For these measurements, forward bias is indicated by current flowing from the large bottom contact through the substrate and into the circular top contacts. Note the symmetric *I–V* for the SiC case, as expected for a homogeneous bulk SiC layer. For the other three cases, asymmetry implies some rectification, attributed to the implantation. Fig. 5 shows the *I–V* data after annealing of the same four regions as in Fig. 4. The presence of Ge and the dopant N yielded much higher currents (lower forward voltage drop) than for the unimplanted diodes. After annealing the current increased the most for the region with only Ge. Breakdown voltages (not shown) for the diodes exceeded the range of the instrument (−50 V).

C–V measurements were performed to extract the built-in voltage, $\Phi_{bi,}$, of the devices. Fig. 6 shows the plots of $1/C^2$ versus voltage for the various regions of the diode wafer. The incorporation of the dopant N increased Φ_{bi}, as one would expect from the difference in E_F across the p–n junctions. The addition of Ge decreased Φ_{bi}, which is reasonable since the bandgap of Ge (0.66 eV) is much smaller than 4H SiC (3.2 eV).

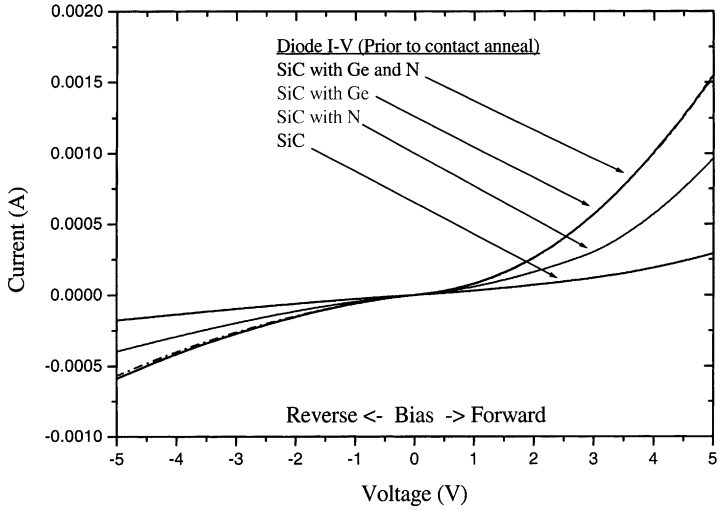

Fig. 4. Electrical (*I–V*) measurements of p-SiC, n-type SiC, p-SiC:Ge, and n-type SiC:Ge, prior to thermal annealing of the metal contacts. The data for SiC with Ge and N is nearly identical to that of SiC with Ge (dashed curve). SiC with N has a substantially larger forward voltage drop, while the pure SiC sample has the largest value of forward voltage drop at a agiven current.

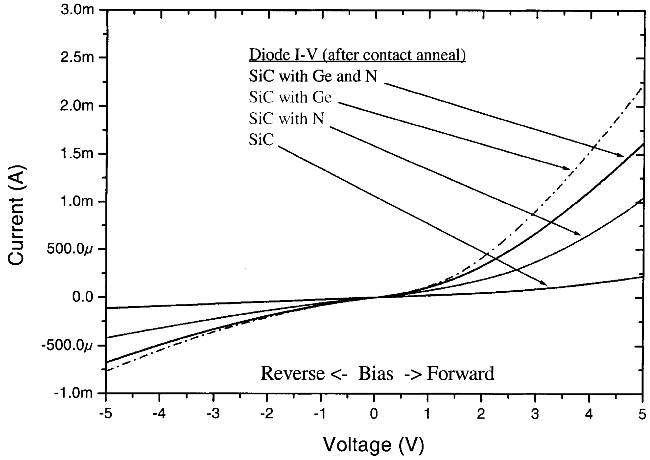

Fig. 5. Electrical (*I–V*) measurements of p-SiC, n-type SiC, p-SiC:Ge, and n-type SiC:Ge, after thermal annealing of the metal contacts. The Ti/Au contacts were thermally annealed in an RTA at 800°C for 1 min in a forming gas environment (85% N and 15% H). Data for SiC with Ge (dashed curve) now has significantly lower forward voltage drop compared to SiC with Ge and N. Again, SiC with N has significantly larger forward voltage drop and the SiC sample shows the largest forward voltage drop at a given current.

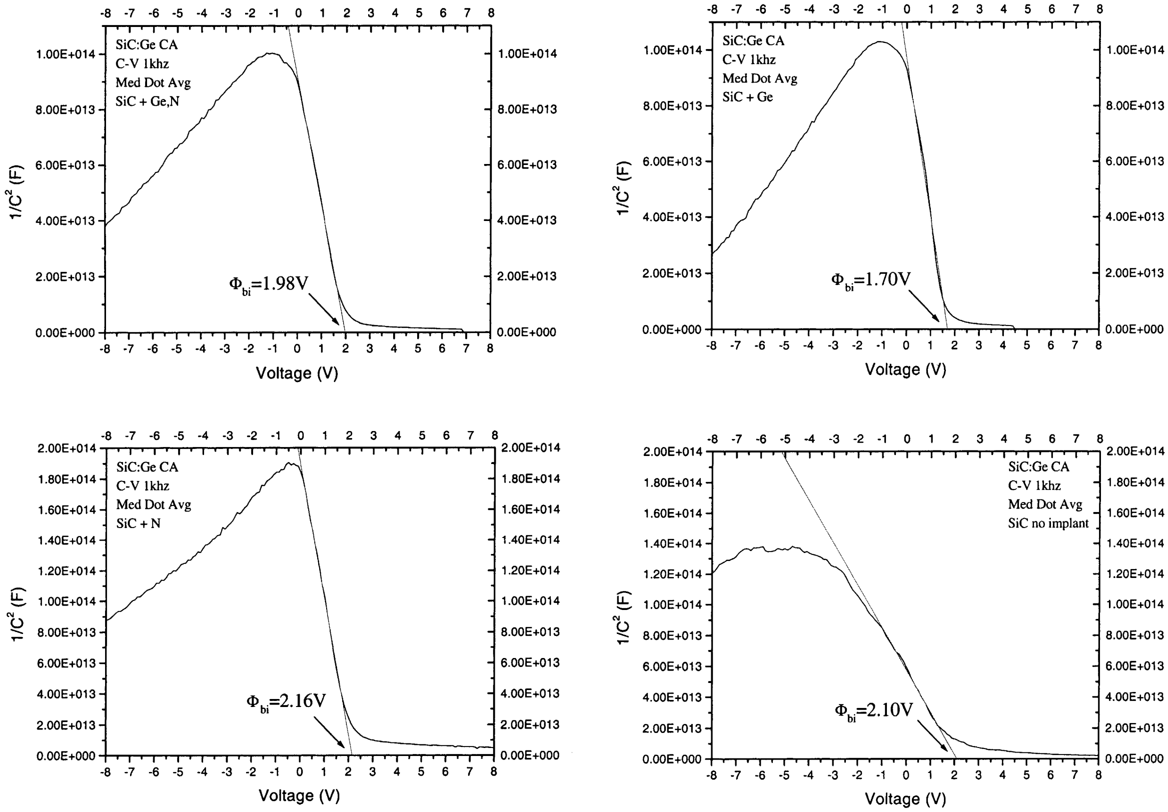

Fig. 6. Capacitance–voltage measurements made of p-SiC, n-type SiC, p-SiC:Ge, and n-type SiC:Ge showing varying built in voltages and a minimum value of built in voltage for the SiC:Ge sample. The built in voltage for the Ge implanted region of SiC showed the lowest value (1.7 V) of built in voltage which was 400 mV less than the built in voltage measured for the SiC sample.

The addition of Ge to SiC caused a 400 mV decrease in the built-in voltage for SiC without N co-doping and a 180 mV decrease for SiC with N, based upon $1/C^2$ plotted as a function of voltage. Since the doping profile is not abrupt, $1/C^3$ verses voltage was also used to estimate the built in voltages (plots not shown). From this analysis the Ge caused the built in voltage to decrease by 100 and 190 mV, respectively, for SiC with and without N.

Electrical contact experiments were carried out to determine how Ge affects the electrical contacts for a p-type SiC wafer. Other researchers have demonstrated the ability to develop reliable electrical contacts with CrB alloys on p-type SiC wafers [4]. Our approach was to evaporate a thin layer of Cr followed by a thicker layer of Ni onto both a SiC sample (p-type without Ge) as well as a p-SiC:Ge sample. The SiC:Ge sample was p-type doped with Al to 3×10^{18} cm^{-3} and implanted with a Ge dose of 8×10^{16} cm^{-2}. The annealing for this implant was performed at 800°C for 1 min. The electrical contacts of both samples were fabricated by thermal evaporation with a chamber pressure of approximately 1×10^{-7} Torr. A thin 500 Å layer of Cr was first deposited followed by 1000 Å of Ni. The metalization structure was a TLM pattern so that contact resistance measurements for both samples could be measured. The *I–V* measurements (Fig. 7) were taken between two adjacent TLM pads for the two samples. The metal contact pads were "as deposited" and not annealed prior to the measurements. The resulting data for the SiC and the SiC:Ge samples are greatly different as shown in the plots of Fig. 7. For the SiC:Ge, the current voltage relation is linear, whereas the *I–V* characteristic of the SiC contact is non-linear and rectifying, characteristic of a metal–semiconductor (MS) junction having a breakdown voltage of approximately 4.2 V. The linear *I–V* behavior for the SiC:Ge sample is attributed to surface states introduced by the Ge implantation process which caused a reduced barrier height between the metal and semiconductor. The reduction of barrier height in Schottky barriers through ion implantation is well documented and has been reported in other works [5]. The total resistance of the metalization on the SiC:Ge wafer was lower than that of the metalized SiC wafer as noted by the current, which is two orders of magnitude larger in the case of SiC:Ge.

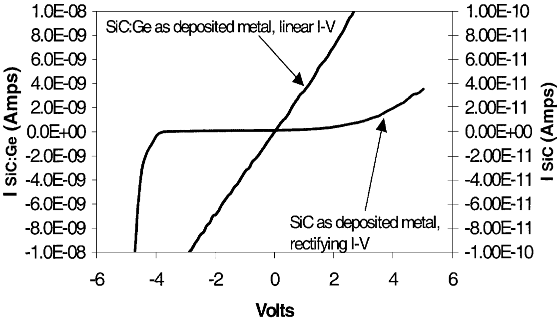

Fig. 7. Electrical (*I–V*) data of SiC and SiC:Ge metal contacts fabricated from Cr/Ni which show an Ohmic contact for the SiC:Ge case and a rectifying contact for the SiC case. The metal contacts were in the form of TLM structures and the measurements were made through adjacent metal contacts on the surface of the samples. All measurements were made with "as deposited" contacts prior to thermal annealing.

4. Conclusions

The effect of Ge ion implantation on the physical properties of silicon carbide substrates has been investigated experimentally to determine possible utilization of the material in heterostructure electronic device applications. The results of the study of a p-type 4H SiC substrate implanted with Ge from a 346 keV ion beam indicate the formation of thin layers of SiC:Ge with approximately 2% Ge concentration. The SiC:Ge had a larger lattice constant than the SiC substrate. XRD data of the SiC:Ge layer showed an X-ray peak near 35.2° compared to the SiC(0004) peak at 35.5°, which implies a Ge content of 2.3% when Vegard's law is assumed. This data is in reasonable agreement with RUMP predictions of 1.6% Ge that was fitted to experimental RBS data of the SiC:Ge sample. The secondary X-ray peak due to Ge incorporation was observed to increase in intensity and shift to a lower Bragg angle as the Ge dose was increased in the SiC:Ge alloy. *I–V* measurements have shown that heterojunction SiC/SiC:Ge devices have a lower forward voltage drop and the lowest contact resistance compared to either SiC or N-doped SiC devices. *C–V* data indicates a lowering of the built in voltage by 100–400 mV for Ge implanted SiC. Cr/Ni electrical contacts have been fabricated onto Ge implanted SiC substrates and were observed to have Ohmic contact characteristics. This was achieved by evaporating directly onto the SiC:Ge layers and prior to annealing.

Acknowledgements

The authors wish to express thanks to the Office of Naval Research (ONR) and the Army Research Office (ARO) who support this research through ONR contract no. N00014-00-1-0834 and ARO AASERT contract no. DAAG55-97-1-0249. The authors also acknowledge T. N. Adam from the Department of Electrical and Computer Engineering, University of Delaware, for technical assistance and review of the final manuscript.

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