Tunneling Injection into Modulation Doping Structures: A Mechanism for Negative Differential Resistance Three-Terminal High-Speed Devices

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***Abstract*—We present a new tunneling injection mechanism into the channel of a modulation doping Field Effect Transistor. In the pre-saturation regime of the drain current, the source current exhibits Negative Differential Resistance as a result of the charge control by the gate field in the channel. The tunneling three terminal device promises high frequency operation.**

CONTINUOUS interest in resonant tunneling (RT) has been stimulated by the expectation of high-speed device operation related to negative differential resistance (NDR) effects [1], [2]. Frequency operation up to 200 GHz has recently been reported in double hetero-barrier diodes [3]. Various attempts have been made to incorporate RT structures into three-terminal (3T) devices, but speed performance has not been reported so far [4]–[8]. On the other hand, high-electron-mobility transistors (HEMT) have demonstrated amplification at 94 GHz, the highest frequency achieved with 3T devices [9]. Real space transfer (RST) structures [10] such as the NERFET also seem to be very promising [11].

We suggest a mechanism of carrier injection into modulation doping (MD) structures, which gives rise to NDR effects controlled externally by a third terminal. The new injection mechanism offers the advantage of combining two fast electronic components—the MDFET and the tunnel junction—into a high-speed 3T device. Fig. 1(a) shows a schematic representation of this composite structure, which we call the tunneling injection FET (TIFET). A thin heavily doped n^+-layer of GaAs is intercalated between a heavily doped p^+-substrate and the undoped (u) region of a conventional MD structure. The (u, n^+)-p^+ junction operates as a backward diode [12] that injects electrons from the substrate (V_{SB} contact) into the two-dimensional (2D) channel. Under equilibrium conditions, the n^+-layer is entirely depleted and forms the junction space charge. The undoped layer contains the 2D electron gas. The additional advantage of a tunnel homojunction is that the p-substrate forms an isolating reverse-biased p-n junction at the source and drain, thereby confining the injection within the active channel region of the MD structure. To avoid tunnel leakage at the contact electrodes, pre-implanted lightly doped n-layers may be used. Notice that the device materials are not limited to the AlGaAs–GaAs system but may include other combinations of III-V compounds such as low-gap InGaAs with InP or InAlAs, for example.

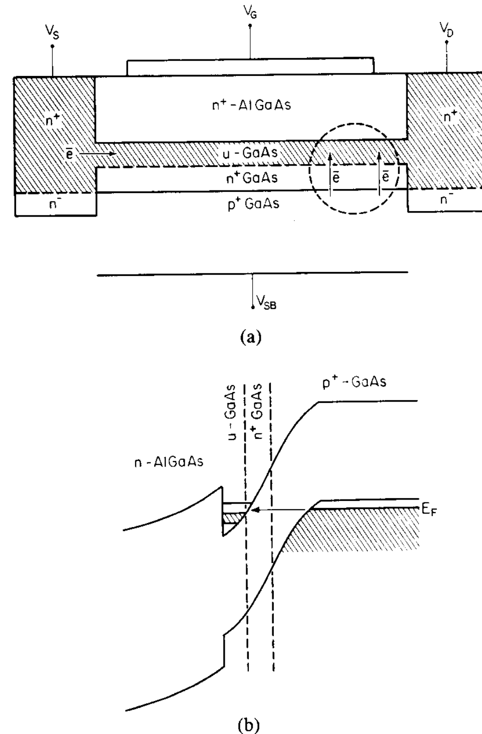

Fig. 1. (a) Schematic representation of the TIFET. The dashed area represents the source and drain contacts as well as the 2-D electron channel. Encircled area shows the predominant tunneling injection region. (b) Cross-sectional energy band diagram of the channel-junction area under reserved bias.

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In its normal mode, the TIFET operates like a MDFET, i.e., the source and the substrate are grounded, and the drain is positively biased. However, owing to the positive voltage distribution in the channel, the tunnel junction is nonuniformly reverse biased and injects electrons into the channel, mostly on the drain side (Fig. 1(b)). Let us now assume two important conditions: 1) the tunnel current is directly injected into the channel without leaking into the source and drain electrodes and 2) the entire channel is in pre-saturation regime (no pinch off). In this condition, the gate field retains control of the channel charge under moderate drain bias, which makes the gradual channel approximation (G.C.A.) [12] valid from source to drain. Let us label the source–drain axis as x; the channel current I_c between two points x and $x + dx$ infinitesimally close is then given by

$$I_c(x + dx) = I_t(x)\,dx + I_c(x) \tag{1a}$$

or

$$dI_c(x) = I_t(x)\,dx. \tag{1b}$$

The integration of the latter relation gives

$$I_D^t = I_c(L) = \int_0^L I_t(x)\,dx + I_s^t \tag{2}$$

where I_s^t and I_D^t are the source and drain currents in the presence of tunneling I_t, respectively, and L is the channel length. The double integration of (1b) yields

$$\int_0^x I_c(x)\,dx = \int_0^x dx' \int_0^{x'} I_t(x'')\,dx'' + I_s^t x \tag{3a}$$

which, using the G.C.A. for $I_c(x) = ZC\mu(V_{GT} - V)\,dV/dx$ and dividing by L results in the useful equation

$$\frac{\mu CZ}{L}\left(V_{GT}V_{DS} - \frac{V_{DS}^2}{2}\right) = \int_0^L \frac{dx}{L} \int_0^x I_t(x')\,dx' + I_s^t. \tag{3b}$$

Here, Z is the gate width, C is the gate capacitance (per unit area), and μ is the electron mobility. V_{DS} is the source–drain voltage and V_{GT} is the effective gate–source bias. The left-hand side of this relation is the expression of the drain–source current I_{DS}^0 in the absence of tunneling. The tunnel current density under reverse-bias can be approximated by the simple relation [12]

$$I_t = ZJ_0\left[(\exp(V/V_t)) - 1\right] \tag{4}$$

where we have neglected the effect of channel quantization in a first approximation. V is the channel–substrate bias, and J_0 and V_t are two constants characteristic of the junction and the tunnel process. The second term in the RHS of (4) accounts for zero bias conditions. Due to its exponential dependence on V_{DS} through $V(x)$, the I_t term in (3b) will increase faster with voltage than the power law I_{DS}^0 term. Therefore, the *source* current I_s^t versus V_{DS} will exhibit an NDR as a result of the combined action of carrier injection into the channel and the control of the total channel charge by the gate field. In some sense, this effect is the inverse-analog of real space transfer [10] since the latter coincide with carrier *ejection* from the channel due to high-energy scattering. The tunnel junction capacitance, which has been neglected in our analysis, does not affect the injection mechanism and consequently does not qualitatively change our conclusions.

Fig. 2 shows a calculation of the source current as a function of the drain voltage for different values of the tunnel current constant J_0. For the sake of simplicity we have assumed that the exponential in the double integral of (3b) is equal to its maximum value. Current and voltages have been normalized for the sake of simplicity. V_t depends on the junction design, but a typical value of 50 mV is not unreasonable, and yields realistic values of the gate bias $V_{GT} = 0.6$ and 1.25 V in the two cases investigated here. At high gate bias, noticeable NDR in the source current occurs in the presaturation regime of the transistor for a wide range of saturation values J_0 (Fig. 2(a)). The smaller the J_0, the steeper the NDR and the higher the peak current, which yields a large peak-to-valley ratio in the I–V characteristics. Therefore, optimum NDR conditions do not require thin excessively doped tunnel junctions since the saturation current J_0 need not be extremely high. This makes the realization of the device feasible with conventional technology. On the other hand at low gate bias, the occurrence of NDR features critically depends on the tunnel saturated current (Fig. 2(b)). With small J_0, the tunnel injection is too weak to substantially influence the source current before the onset of normal current saturation in the channel. With large J_0, tunneling dominates and the FET action is lost; the source current ceases to be controlled by the gate field.

Consequently, for a particular junction design with given J_0 value, the gate bias can then be used to turn the NDR on or off by controlling the source current injection. The device operates as a switch for the NDR.

The speed performance of the TIFET is essentially determined by the time constants associated with the tunneling time and the channel charging time. The former is a function of the level broadening ΔE resulting from the interaction between electronic states across the junction [13]–[15], i.e.

$$\tau_{\text{tun}} = \pi\hbar/\Delta E.$$

In heavily doped junctions ($N_D \sim 10^{19}/\text{cm}^3$) of small-gap materials such as InGaAs ($E_G \sim 0.75$ eV), the maximum electric field $F_{\max}$ exceeds 10^6 V/cm. In strong reverse bias, the tunneling distance can decrease below 50 Å, which is comparable to the barrier width used in heterojunction RT. The typical energy level broadening resulting from the interaction between electronic states across the potential barrier is of the order of 1 meV [15] so that τ_{tun} can be as low as 2 ps. The channel charging time is given by the carrier transit time, which is actually limited by the saturation velocity V_{sat} [12], i.e.

$$\tau = \frac{L}{V_{\text{sat}}} \sim 1 \text{ ps}.$$

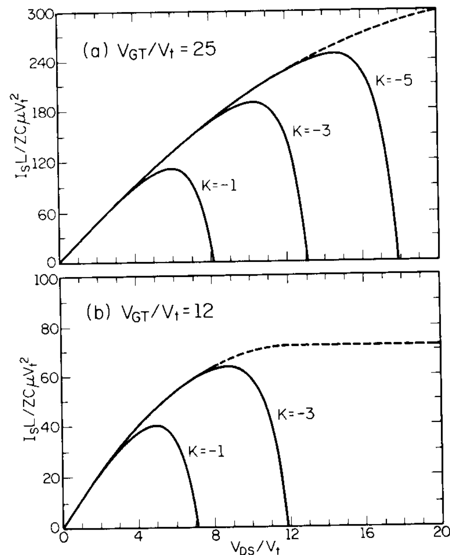

Fig. 2. Normalized I-V characteristics of the source current for various injection conditions. Curves have been interrupted at the onset of saturation, i.e., for $V_{GT} = V_{DS}$.

$$K = \log_{10}\left(\frac{J_0 L^2}{C\mu V_t^2}\right)$$

is the tunnel injection parameter. Dashed line: $J_0 = 0$.

Therefore, for a quarter-micrometer gate length, the resulting limiting time that determines the speed of the TI-FET is of the order of a few picoseconds and promises operation in the 100-GHz range.

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