

# Artificial Dendritic Trees

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## Abstract

The electronic architecture and dynamic signal processing capabilities of an artificial dendritic tree which can be used to process and classify dynamic signals is described. The electrical circuit architecture is modeled after neurons that have spatially extensive dendritic trees. The artificial dendritic tree is a hybrid VLSI circuit and is sensitive to both temporal and spatial signal characteristics. It does not use the conventional neural network concept of weights, and as such it does not use multipliers, adders, look-up-tables, microprocessors or other complex computational units to process signals. The weights of conventional neural networks, which take the form of numerical, resistive, voltage, or current values, but do not have any spatial or temporal content, are replaced with connections whose spatial location have both a temporal and scaling significance.

## 1.0 Introduction

Interest in using artificial neural networks for the identification and control of dynamical systems is growing (e.g. Narendra and Parthasarathy, 1989). However, most neural network models do not include spatiotemporal dynamic signal processing capabilities. In these models, the neuron is treated as a point entity that receives and processes inputs at the soma, which makes spatial signal processing difficult or impossible. In our modeling approach, we have looked beyond the soma to the extensive dendritic tree structure of neurons, which not only forms most of the cell's surface area but provides spatiotemporal signal processing capabilities not present in models which assume a point-entity neuron.

The artificial dendritic tree described in this paper is a hybrid circuit and is sensitive to both temporal and spatial signal characteristics, but it does not use the conventional neural network concept of weights, and as such it does not require multipliers, adders, look-up-tables, or other complex computational units to process signals. The weights of conventional neural networks, which take the form of numerical, resistive, voltage, or current values, but do not have any spatial or temporal content, are replaced in our system with connections whose spatial location have both a temporal and scaling significance.

We have only recently begun to experiment with networks of artificial dendritic trees (Elias, 1992a). We have fabricated and tested artificial dendritic branches in CMOS analog VLSI (Elias et al., 1992), and we have used a genetic algorithm to train simple networks to follow a maneuvering target that moves in one dimension (Elias, 1992b). The research described here attempts to capture neurocomputational principles by applying structure and behavior modeled after synaptic and dendritic levels of biological implementation. We hope to demonstrate that electronic analogs of biological computational devices, that include the properties of spatially extensive dendritic trees and the impulse response of chemical synapses, can form the basis for powerful artificial neurosystems.

## **2.0 Artificial Dendrite and Chemical Synapse**

In this section, we describe electronic circuits that 1) emulate the electrical behavior of passive dendritic trees and chemical synapses and 2) are simple and robust enough to ensure that networks, which ultimately need to support huge numbers of synapses, can be constructed with standard VLSI processing. Electronic analogs of active dendrite behavior (e.g. Llinas and Sugimori, 1980; Shepherd et al., 1985, 1989; Hounsgaard and Midtgaard, 1988) will not be treated in this paper.

## 2.1 Artificial Dendrite

Passive artificial dendrites are formed by a series of standard compartments, where each compartment has a capacitor,  $C_m$ , that represents the membrane capacitance, a resistor,  $R_m$ , that represents the membrane resistance, and an axial resistor,  $R_a$ , that represents the cytoplasmic resistance (e.g. Rall, 1989). Figure 1a shows a section of artificial dendrite with five standard compartments that is part of a much longer branch like that shown in figure 1b.

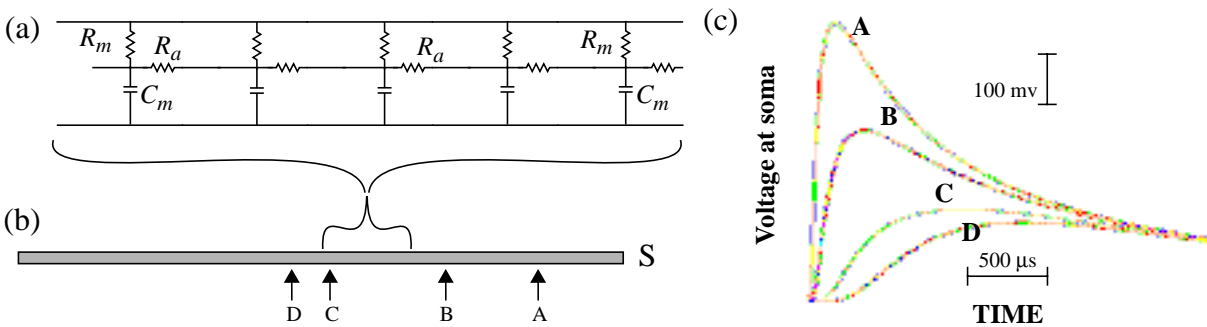


FIGURE 1 a) Compartmental model of passive dendrite. Each RC section,  $R_m$ ,  $R_a$ , and  $C_m$ , is a standard compartment that simplifies VLSI layout. b) Standard compartments are abutted on substrate to form silicon dendritic branches. c) Impulse response of single artificial dendritic branch due to transient transmembrane current at indicated locations on branch.

The transient response of the artificial dendrite is of primary importance. Figure 1c shows the impulse response measured at point  $S$  due to inward impulse current at four different locations,  $A$ ,  $B$ ,  $C$ , and  $D$  on a passive artificial dendrite as represented in figure 1b. The location  $S$  represents the position of the soma. Therefore, the voltages measured at  $S$  are those that would affect somatic voltage-sensitive circuits and perhaps cause the generation of an efferent impulse. As with biological passive dendrites, the peak voltage amplitude is largest for transmembrane current nearest the soma and gets rapidly smaller for sites further away. The time for the voltage to peak shows a similar behavior: time-to-peak-voltage increases with distance from  $S$  (e.g. Rall, 1989). The behavior shown in figure 1 illustrates how the concept of weight is an inherent property of the dendritic physical structure. It is clear that position along the artificial dendrite can be used to produce an effective weighting, in both time and amplitude, of afferent signals that are in the form of a transient inward or outward current.

## 2.2 Artificial Chemical Synapse

The means for enabling inward or outward impulsive current at a specific artificial dendrite location is accomplished by using a single MOS field effect transistor. A p-channel transistor enables inward current, which produces an excitatory type response, and an n-channel transistor enables outward current, which results in an inhibitory type response. The complete artificial dendrite circuit is shown in figure 2a, where both p-channel (upper) and n-channel (lower) transistors are placed at uniform positions along the branch. The transistors are turned on by an impulse signal applied to their gate terminals. Both transistor types operate in the triode region (e.g. Allen and Holberg,1987). Therefore, the amount of transmembrane current depends on the conductance of the transistor in the on state, the duration of the gate terminal impulse signal, and the potential difference across the transistor, which is dependent on the state of the dendrite at the point of the synapse. All excitatory transistors have identical drawn dimensions (as do inhibitory transistors), and both excitatory and inhibitory artificial synapses are placed at the same locations in the current chip implementation. It is possible that after further system level experimentation, we may find that a different synapse distribution is preferred.

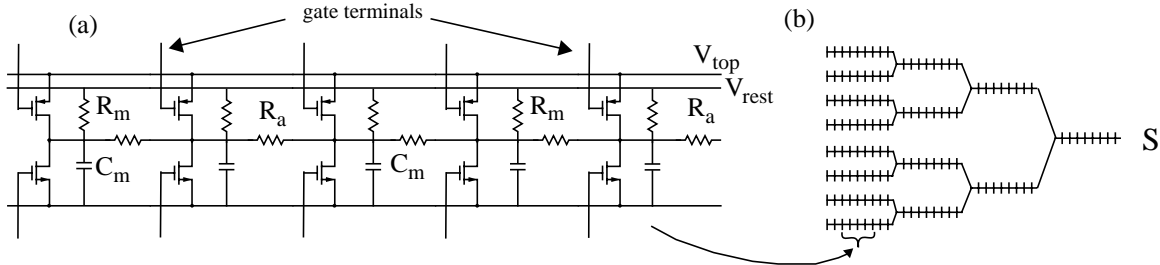


FIGURE 2 a) A five compartment section of artificial dendrite with five excitatory and five inhibitory artificial synapses.  $V_{rest}$  is the resting voltage,  $V_{top}$  is the maximum membrane voltage. (b) A multibranched artificial dendritic tree which is constructed by piecing together artificial dendrite sections like that in (a).

## 2.3 Electrical Response of Artificial Dendritic Trees and Synapses

In figure 1, we illustrated the behavior of the impulse response amplitude as a function of the synapse position on the artificial dendritic tree, thus demonstrating the effective weighing of inputs that are mapped onto the tree structure. The impulse response amplitude as a function of the afferent impulse signal width is shown in figure 3a, which represents measured responses from

one of our VLSI circuits for four different impulse widths. A similar postsynaptic behavior is found in biological preparations under presynaptic voltage-clamp: presynaptic depolarization produces a nearly linear increase in postsynaptic voltage (e.g. Angstadt and Calabrese, 1991). This behavior may be due to a lengthening of the time over which transmitter is released, thereby increasing transmembrane current in the postsynaptic terminal. In any event, the efficacy of existing connections in our system can be changed by altering the impulse width. We are investigating how this may be done on a local basis, perhaps consistent with Hebb's postulate (Hebb, 1949), such that both local synaptic strength and the location of the synapse on the branch combine to produce an effective synaptic weight for a given connection.

The artificial dendrite's voltage response to closely spaced impulses is shown in figure 3b. The response due to each synaptic event is added to the resultant branch point voltage from past events until the voltage reaches a maximum value. This behavior is the expected impulse response of an Nth-order system and is solely due to the effective postsynaptic membrane. The same behavior would be observed if the phasing of multiple, transiently conducting, artificial synapses was short compared to the effective membrane constant. An example that utilizes this behavior is discussed in section 4.

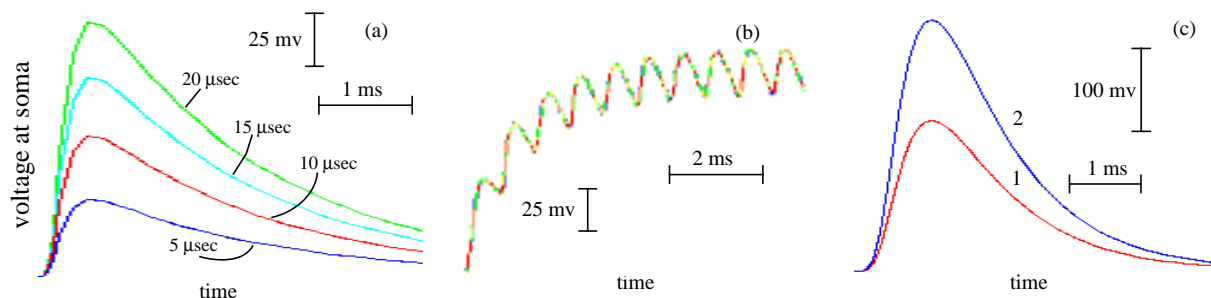


FIGURE 3 Experimental results from artificial dendrite-synapse circuit to afferent stimulation a) Graded response: amplitude of voltage peak at soma is linearly related to afferent impulse width over wide range. b) Tetanus response: closely spaced impulses cause voltage response to saturate. if impulse rate is faster than membrane decay time c) Nonlinear and nearly-linear response: curve 1 is the resultant somatic voltage for simultaneous stimulation of two adjacent synapses on same branch (see fig 2b). Curve 2 is somatic voltage for simultaneous stimulation of two synapses on different branches. Positions of synapses for curves 1 and 2 were equidistant from soma.

Multiple, simultaneously conducting synapses that are electrically close together produce a voltage at the soma that is less than the sum of their individual responses (e.g. Shepherd and

Koch, 1990b). This sublinear effect is due to the shunting load seen by each synaptic site when electrically nearby synapses open their channels. In contrast, multiple, simultaneously conducting synapses that are electrically far apart produce a nearly linear resultant voltage at the soma. Both of these behaviors, as measured at the trunk of a two-branched artificial dendritic tree (e.g. point S in figure 2b), are shown in figure 3c. The smaller voltage transient (curve 1) was measured when two adjacent artificial synapses were simultaneously active on the distal end of one of the branches. The larger voltage transient (curve 2) shows the resultant voltage when two artificial synapses on separate branches were simultaneously active. In this case, the resultant is nearly twice that of the previous example. In both cases, the artificial synapses were equal distance from the point of measurement. This type of behavior clearly enriches the signal processing capabilities of systems comprised of spatially extensive dendritic trees (Koch and Poggio, 1987).

### 3.0 Silicon Dendritic Trees

If artificial dendrites are to be used in real systems then they must be implemented via a process that can make huge numbers of them in a small area inexpensively. The only feasible path for doing this currently is with standard silicon processing methods (e.g. Mead, 1989). In this section, we discuss briefly the implementation of a dendritic system in silicon.

#### 3.1 Convergent, Divergent, and Recurrent Connections

Networks that are built with artificial dendrites and synapses process signals that have a spatiotemporal significance by mapping afferent signal pathways to specific locations on the dendritic trees. The connections between synapses and the outputs of sensors and neurons determine the overall system response for a given dendritic dynamic behavior. The number of different connection patterns is quite large and is a factorial function of the number of synapses and sensor elements. If we limit, for the moment, the number of divergent connections to one, then the total number of different connection patterns is given by

$$\frac{N!}{(N-M)!} \quad (1)$$

where  $N$  is the number of artificial synapses and  $M$  is the number of sensor and neuron outputs. Artificial systems may have thousands of afferents and many times more synapses, resulting in an extremely large number of possible connection patterns. In our system, we allow each sensor element or artificial neuron to make unrestricted divergent connections and each synapse to receive multiple convergent connections from both sensor elements and artificial neurons. This tends to make the number of possible connection patterns much larger than that indicated by equation (1).

### **3.2 Virtual Wires**

In the implementation of an electronic system, the number of data pathways in or out of modules is limited by the available technology. Integrated circuit packages rarely exceed 500 pins; our current artificial dendrite chip is in a 40 pin package. This limitation in pin count is of special concern with dynamic artificial neuronal systems because of the analog nature of the computation. Each sensor or neuron output must be able to connect to any one of the artificial synapses in the system, and the spiking outputs from sensors and neurons must arrive at their artificial synapse destinations in a parallel fashion.

In order to overcome I/O limitations and to meet the connectivity and timing requirements, we make use of a multiplexing scheme that we refer to as virtual wires. In this scheme, the outputs of active neurons and sensors (i.e. those that are currently producing a spike or impulse) cause the synapses that they connect with to become activated after a delay that is specific for each efferent connection. The process of reading an active output causes that output to return to the inactive (i.e. nonspiking) state. After all sensor and neuron output states have been sampled, the activated synapses throughout the system are turned on transiently by a global impulse stimulus signal. The process of determining active sensors and artificial neurons, delayed activation of synapses that connect to active sensors and neurons, and transiently turning on active artificial synapses continues indefinitely with a period that depends on system dynamics.

Virtual wires are formed using four digital circuits: Stimulus Memory, which is closely

associated with each synapse, Address Decoding, which serves all on-chip synapses, State Machine, which determines sensor and neuron output states, and Connection List, which specifies the locations of synapses and the axonal delay associated with each connection. Stimulus Memory and Address Decoding are on-chip circuits; the Connection List and State Machine are off-chip.

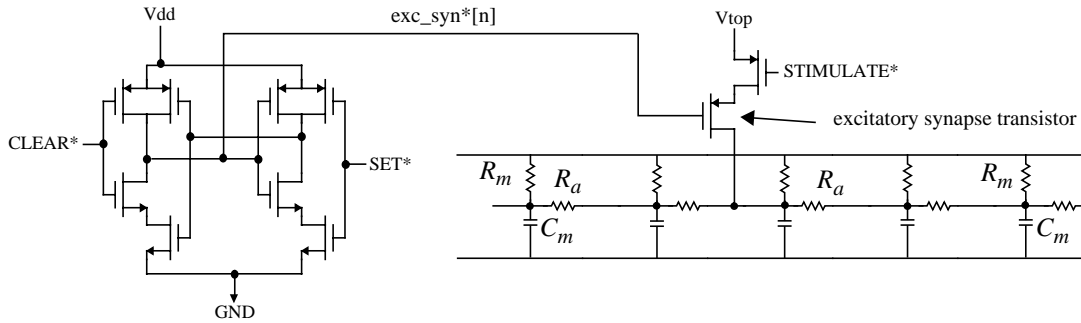


FIGURE 4 Circuit diagram of one of the excitatory Stimulus Memory registers shown with its p-channel excitatory synapse transistor. When SET\* is asserted the synapse is activated (i.e. exc\_syn\*[n] is set to logic 0) and the artificial synapse will turn on when STIMULATE\* is asserted. CLEAR\* inactivates all Stimulus Memory locations throughout the system. Both STIMULATE\* and CLEAR\* are global signals in the system.

The circuit diagram of an excitatory Stimulus Memory register connected to its p-channel artificial synapse transistor is shown in figure 4. In the current implementation, virtual wires add nine transistors to each artificial synapse. A synapse is activated when its exc\_syn\*[n] is set to logic 0 by asserting SET\* while CLEAR\* is unasserted. The SET\* signal is asserted by the on-chip address decoder when the proper combination of external address lines and control signal are asserted. An activated synapse will turn on when the global impulse signal, STIMULATE\*, is asserted. The global signal CLEAR\* is asserted after every STIMULATE\* assertion to inactivate synapses in preparation for the next round of sampling and activation.

The Connection List is a multiple-bit-wide memory that holds the synapse addresses and axonal delay of each efferent connection in its domain. For large systems, we plan to divide the network into domains that will permit a certain level of parallel sampling of neuron and sensor outputs which should enhance system scalability. The Connection Lists across all domains hold the pattern of connectivity for the system and thus their contents determine system behavior. A connection pattern can be fixed in ROM, or as in our present system, loaded via computer for

experimentation.

Figure 5 illustrates a simplified single-domain system comprising Connection List, sensor, State Machine, and four neuromorphic chips, each of which contain a number of artificial neurons. The outputs of the artificial neurons on each chip are sampled via a multiplexer which is selected by the on-chip address decoder. Each neuron is in one of two states, so only a single output pin is needed to read all of them. In operation, the State Machine reads the state of each sensor element and every neuron in its domain. A spiking neuron or sensor output is detected by the State Machine which then activates all of the synapses that connect to that particular sensor or neuron. After reading all outputs, STIMULATE\* is asserted transiently, thus briefly turning on activated synapses. This is followed by asserting CLEAR\*, which inactivates all synapses. As with Mahowald's method of connecting neuron outputs to synapses (Mahowald, 1992) addresses of synapses and neurons are used rather than direct connections carrying spikes.

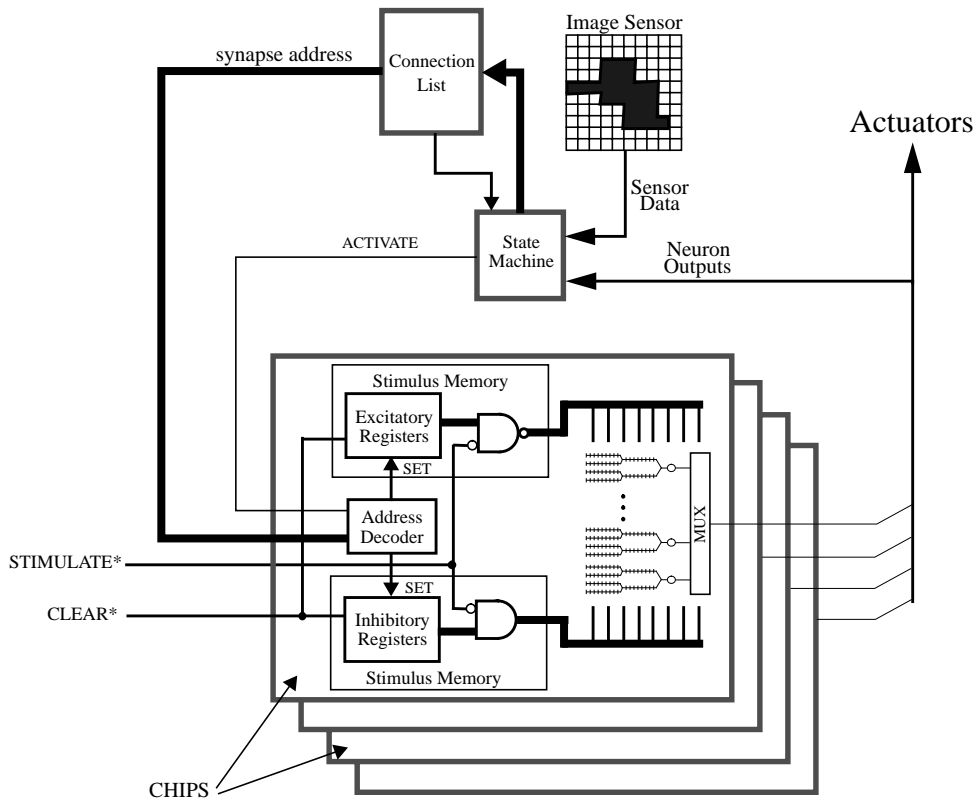


FIGURE 5 Simplified block diagram for single domain system showing basic operation. All sensory and neuronal outputs simultaneously activate the artificial synapses that they connect to through the virtual wires.

### 3.3 Standard Dendrite Compartment

Figure 6 illustrates the basic integrated circuit layout of our standard dendrite compartment. Each compartment has a capacitor,  $C_m$ , that represents the membrane capacitance, a resistor,  $R_m$ , that represents the membrane resistance, and an axial resistor,  $R_a$ , that represents the cytoplasmic resistance. For the results reported here, the size of the artificial dendrite standard compartment was  $18\ \mu\text{m}$  by  $180\ \mu\text{m}$  with most of this area being taken up by the capacitor.

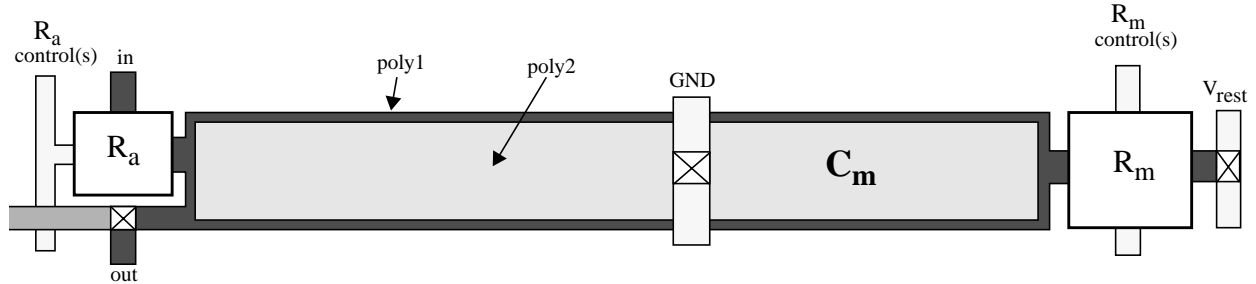


FIGURE 6 Basic VLSI layout for standard dendrite compartment. Control lines for resistors permit adjustment of resistance over a limited range.  $V_{rest}$  establishes the resting voltage (typically 1V).

The capacitor is the largest element in the standard dendrite compartment and is implemented using conventional silicon processing methods (e.g. Allen and Holberg, 1987). The capacitor was fabricated with two layers of polysilicon separated by a thin oxide layer. The top plate of the capacitor is polysilicon layer 2 (poly2) and connects to a ground bus that runs perpendicular to the long axis of the capacitor. The bottom plate is polysilicon layer 1 (poly1) which connects directly to the resistors,  $R_a$  and  $R_m$ , and to the synapse transistors in the stimulus memory (see figures 4 and 6). The capacitance for the current size standard compartment capacitor is approximately 1 pf, which is based on an oxide thickness of approximately  $700\ \text{\AA}$ . There are many techniques to reduce the footprint of the capacitor while keeping the same capacitance: thinner dielectric, use material with a higher dielectric constant, e.g. silicon nitride, employ three-dimensional capacitors, e.g. trench or tower capacitors, but we will not explore these further here.

The compartmental resistors may be implemented by a number of standard silicon fabrication techniques: well, pinched, active, and SC (e.g. Allen and Sanchez-Sinencio, 1984). The resistor footprint for a particular resistance depends not only on the resistance value but also on the

implementation technique. Well resistors are made by  $n^-$  or  $p^-$  diffusion and have a footprint advantage over the other techniques because the well resistor can be put under the capacitor. Therefore, a well resistor does not take up any silicon real estate but it has the disadvantage of relatively small resistance (measured as  $5 \text{ k}\Omega$  per square for our chips). Pinched resistors have a higher resistance but can not be placed under the capacitor. Active and SC resistors are made from MOS transistor circuits that are designed to emulate resistor behavior over a certain range of terminal voltages and resistance values.

We have implemented n-well, active, and SC resistors on different chips and will report on the details of their design and relative behavior later (Elias and Meshreki, 1993). In our standard dendrite compartment, n-well resistors go under the capacitor and active or SC resistors are placed at the ends of the capacitor as shown in figure 6. Independent control signals for changing the resistance of the SC or active  $R_m$  and  $R_a$  pass along both sides of the compartment. For chips with active resistors, the control signals are DC voltages that permit a certain range of adjustment. With SC resistors, the control signals are AC voltages in which the frequency determines the resistance. Presently, the  $R_m$  resistors in all of the compartments share the same control signals and the  $R_a$  resistors share a different set of control signals. Therefore, all compartments have nominally the same  $R_m$  and  $R_a$  resistances.

The standard dendrite compartment was designed to abut with adjacent compartments and was pitch-matched to the on-chip virtual wire circuitry. This method makes the construction of artificial dendritic trees a relatively simple task: to make a branch, standard compartments are placed side-by-side until the desired branch length is reached. Branches are then connected via metal or poly wires to form trees. The spacing between compartments is the minimum distance between capacitors ( $2 \text{ }\mu\text{m}$ ). The compartments are aligned such that the inputs of one compartment connect to the outputs of the previous compartment.

### 3.4 A Simple Silicon Implementation

The artificial dendritic tree circuit and its on-chip virtual wiring was fabricated using a 2  $\mu\text{m}$  CMOS double-poly n-well process on a 2mm by 2mm Mosis Tiny Chip (e.g. Mead, 1989). The artificial somata and output multiplexer were left off the chips to permit experimentation with different soma circuits. Four artificial dendritic branches each having 15 excitatory and 15 inhibitory artificial synapses were implemented on the chip. The number of synapses was kept low in order to leave open silicon areas on the chip for other analog test circuits.

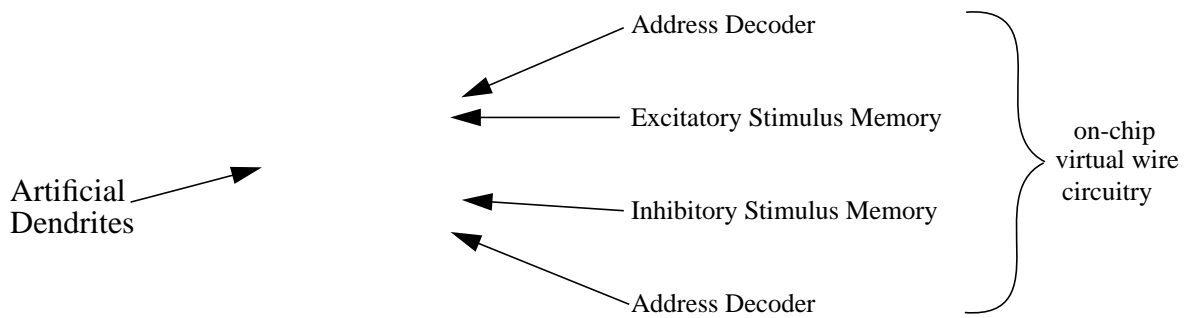


FIGURE 7 Chip layout of artificial dendrites fabricated using a MOSIS 2  $\mu\text{m}$  double polysilicon standard CMOS process. The four artificial dendritic branches can be seen in the center of the die. The ends of each branch are connected to pads which allows experimentation with different branching structures. Each branch has 30 synapses (15 excitatory and 15 inhibitory) which are uniformly spaced along the branch.

Figure 7 shows the complete artificial dendrite chip layout. In the current implementation, the four branches are in-line, with a gap in between each branch, and centered on the die. The ends of each branch are taken out of the chip through package pins to allow experimentation with different tree structures. Multiple chips can be combined as well to produce tree structures with more branches, longer branches, or higher order branching. The remaining circuitry makes up the virtual wires. We are currently working on several new chip designs that we expect will reduce the silicon area needed for the on-chip virtual wires. We are also investigating the addition of shunting inhibition as well as local synaptic weight storage that could be used to modify the effective weights of existing connections.

## 4.0 Simple Test Circuits

Three simple, artificial dendritic tree experiments, two of which do not make use of temporal aspects of dendritic trees, are described next. In each experiment, the output shown represents the measured branch node voltage from one of our circuits for a period of time after the tree received impulsive afferent sensory signals. The sensory signals for each experiment were generated by a computer and were applied to the artificial synapses through a parallel interface. The sensor elements were set to a logic one if the sensor field was above a fixed threshold voltage and a logic zero otherwise. In each experiment, a sequence of sensor data over time was presented to the tree and the resultant waveform was captured with an 8-bit digitizer. Although binary level, one-dimensional sensor data were used, each test circuit would produce similar results with multilevel, two-dimensional sensor data, albeit with different connection patterns and branching structure.

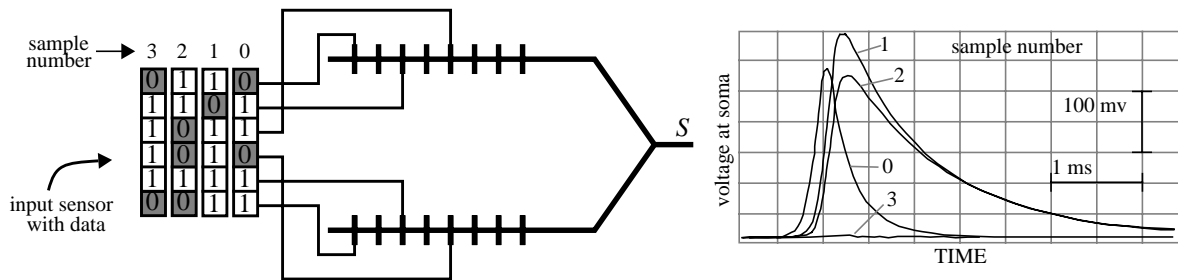


FIGURE 8 Input sensor with six elements connected to dual-branch artificial dendritic tree. The connection pattern shown, classifies input patterns into symmetric and asymmetric classes. The sensor, with its data field, is shown at four different times, the last having a symmetric data pattern. Symmetric data fields result in a null output. Asymmetric sensor data fields produce either a positive or negative voltage trajectory. The output for the four sample times are shown at the right which represents measured data from one of our circuits. Excitatory artificial synapses are top connections on each branch. Inhibitory artificial synapses are bottom connections.

Sensor elements that are a logic one at time,  $t$ , cause an impulse signal to be applied to the gate terminals of the artificial synapses that they connect to through the virtual wires. Therefore, active sensor elements (i.e. those that hold a logic 1 at time  $t$ ), cause their respective artificial synapses to turn on transiently. Inactive sensor elements (i.e. those that hold a logic zero at time  $t$ ) do not cause any artificial synapses to turn on.

Figure 8 illustrates how a two-branched artificial dendritic tree can detect asymmetric patterns in the sensor field. In this experiment, the sensor had 32 elements, but only six elements are shown here for simplicity. The same results would be obtained with virtually any size linear sensor array. The center of the sensor array represents the plane of symmetry, and the connections for a particular branch go only to sensor elements on one side of this plane. In this example, the top branch has one inhibitory and two excitatory connections. The bottom branch has one excitatory and two inhibitory connections. This connection pattern is not the only one that produces acceptable output. In general, there may exist a large number of connection patterns that produce acceptably good results.

The sensor contents are shown at four different times, one of which contains a symmetric pattern. Not shown in the figure are the two trivial cases in which all elements are either logic one or logic zero. Both of these are symmetric and produce no output transient voltage. The case in which sensor elements are all ones, activates all artificial synapses which are connected to these sensor elements, and the resultant signals sum approximately to zero at the branch point. Each connection from one side of the sensor plane of symmetry is mirrored with an opposite polarity connection on the other side that is equidistant from the branch point. When there is an asymmetric sensory pattern, as for sample numbers 0-2, there exists an imbalance between the activated artificial synapses, which results in a transient voltage at the branch point.

Figure 9 shows an experiment that follows an analysis of temporal processing in dendrites by Rall (Rall, 1964). In this example, adjacent excitatory artificial synapses on one branch are connected to adjacent sensor elements. In this experiment, the sensor had 15 elements, but only eight elements are shown for simplicity. This simple connection pattern produces an output that is sensitive to the direction and speed of a moving target. Figure 9a shows the resultant branch point voltage for an eight segment time series in which a target moves across the sensor array from right to left. The target, in this case, is a logic one. The branch point voltage transients occur as the target moves across the sensor field, as can be seen in the plot of voltage vs. time. In figure 9a, the

artificial synapse nearest to the branch point is stimulated first and later followed by the stimulation of the next more distal synapse. The effect is that the resultant voltage transients arrive at the branch point well separated in time and therefore do not overlap significantly. In figure 9b, the target moves from left to right. In this case, the most distal artificial synapse is stimulated first and followed later by stimulation of the more proximal synapses. The resultant voltage at the branch point is larger than it was for the case when the target moved in the opposite direction because the arrival times of the individual transients are more closely aligned. The classification of target direction is then completed by a simple comparator.

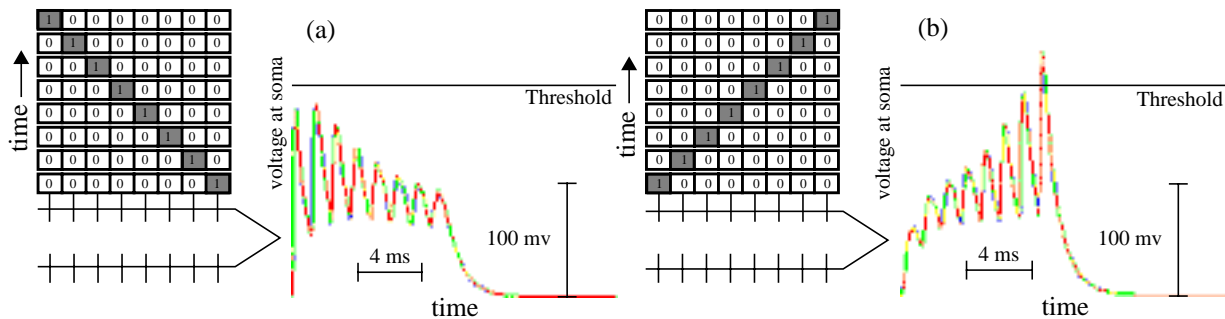


FIGURE 9 Experiments showing the target-direction capabilities of dendrites (after Rall, 1964). a) Target (shaded sensor element) moves from right to left across sensor array. Resultant waveform is lower in peak voltage than in (b) where target moves from left to right. A simple thresholding device classifies target direction.

Figure 10 shows a simplified circuit diagram that uses a single branch of artificial dendrite to provide a control signal for a maneuvering-target tracking application (Elias, 1992c). The sensor, in this example, is a threshold device with seventeen elements, each of which outputs a one or a zero. In figure 10, the one-dimensional sensor pattern over time is that of a simple maneuvering target, which, in this example, is a logic zero on a background of logic ones. In general, the target could be of any shape as long as it was distinguishable from the background.

When the target is on center, the output of the dendritic branch is approximately zero. This is because all excitatory and inhibitory artificial synapses are simultaneously conducting, thereby cancelling each other. Small variations in target position around the center produce relatively small output voltage transitions which can be used for low gain system control. If the target moves

below center, as shown in figure 10, the resultant voltage transients are positive. If, however, the target moves above center, the transients are negative. As the target moves farther off center, either above or below, the resultant branch output peak voltage rapidly increases. This occurs because more proximal artificial synapses turn on, which, in effect, shifts the system control to higher gain. The relative amplitudes of the branch output voltage transients as a function of the distance between target and sensor center can be arbitrarily set by moving connections of particular sensor elements to either more distal or more proximal artificial synapses (Elias, 1992b).

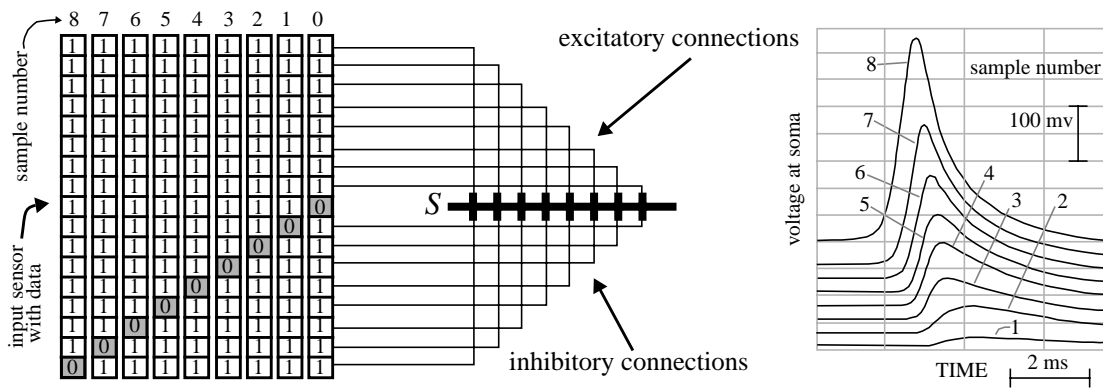


FIGURE 10 Input sensor with seventeen elements connected to a branch of an artificial dendritic tree which responds to the position of a target in the sensor array. The connection pattern shown, produces a dynamic response that depends nonlinearly on how far off the target is from the center. When the target is centered, the output (at  $S$ ) is a null. As the target moves off center, the resultant voltage increases rapidly with separation distance between target and center. The sensor, with its data field, is shown at nine different times. Each sample time shows the target (in this case a 0) going off center and the resultant output (offset for clarity) from the artificial dendritic branch. The top half of the sensor array connects to only excitatory artificial synapses. The bottom half connects only to inhibitory synapses. The resultant voltage transients at  $S$  were captured using an 8-bit digitizer.

## 5.0 Summary and Discussion

In our research program, we have adopted Mead's methodology (Mead, 1989) for implementing neuromorphic systems: 1) study the relevant biological implementation; 2) extract the important computational principles; 3) make optimum use of the inherent properties of electronic devices; and 4) implement, using standard silicon processing techniques. In the work reported here, we have studied the properties of both active and passive biological dendritic trees as well as the dynamic and static behavior of chemical synapses. We have extracted principles of

computation exhibited by passive dendrites with chemical synapses and have translated these principles to a simple and scalable electronic form implemented in standard CMOS technology.

Although our electronic models of chemical synapse and passive dendritic tree are, in many respects, extreme simplifications of biological structures, their dynamic electrical behavior appears to satisfactorily follow that of their biological paragons. The artificial dendritic tree structure is based on a current understanding of passive dendritic trees which results in an extremely simple circuit implementation that is highly scalable. Artificial neurons with extensive dendritic trees have the capability to process signals that have both temporal and spatial significance. In our networks, weights are replaced with connections which, when combined with the sublinear behavior of electrically close synapses and the nearly linear behavior of widely separated synapses, provide a rich computational substrate for signal processing.

## 6.0 Acknowledgments

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