

Chapter Three

Silicon Dendritic Trees

John G. Elias

University of Delaware

INTRODUCTION

In the vertebrate nervous system, communication between distant neurons is done using encoded pulse streams. Closely packed neurons may not produce impulses at all, relying instead on electrotonic spread of membrane potential differences to communicate (e.g. McCormick, 1990). Impulses are also used within the dendritic trees of some, or perhaps all, spatially extensive neurons (e.g. Llinas and Sugimori, 1980). However, their role is not well understood, partly because experimental measurements are extremely difficult to obtain within thin dendritic branches.

Although long distance communication needs may have been the primary evolutionary force behind encoded pulse streams, their impact goes well beyond simple communications. Neurons are continuously bombarded by hundreds or thousands of afferent pulse streams whose impulse responses are integrated by the cell's active and passive membrane elements. A cell's response depends on, among other things, its morphology, membrane electrical and chemical properties, and the location of afferent synapses. The resulting membrane voltage trajectory due to the integration of individual impulse responses plays a critically important role in the dynamic behavior of the cell (e.g. Rapp et. al., 1992). Even a relatively small number of afferent pulse streams leads to complex changes in membrane voltage that may be useful in neural computation (e.g. Northmore and Elias, 1993).

As pointed out by Murray et. al. (1987, 1991), the use of encoded pulse streams for computation and for communication represents an attractive approach towards implementing highly robust large-scale artificial neuronal systems. In their approach, binary signals in the form of encoded pulse streams are used to control analog circuitry and carry information between computational units. The pulse coded approach has since been adopted by a number of research groups, some of which are represented by chapter contributions in this book.

In this chapter, we describe the silicon implementation of an ADT (artificial dendritic tree) that is intended to emulate the behavior of spatially extensive biological neurons which have passive dendrites. We begin with a presentation of background material that should illustrate the linkage between our artificial structures and their biological paragons. This is followed by a description of the artificial neuronal elements and their behavior under impulse excitation. The next section covers aspects of silicon implementation, and the final section is a brief discussion of a tracking controller that makes use of ADTs.

BIOLOGICAL COMPUTATIONAL ELEMENTS

Neuron anatomy can be generalized as having three major parts with the following highly simplified functional descriptions: 1) a spatially extensive dendritic tree, which receives and integrates afferent signals at specific synaptic sites distributed over the entire tree structure; 2) a soma, which forms a response based on the collective dendritic tree electrical signal; and 3) an axon, which propagates efferent impulsive signals from the soma to distant dendritic trees of other neurons. All parts of the neuron depend with varying degree on electrical and chemical changes elsewhere in the cell. For many neurons, the dendritic tree occupies 80-90% of the total surface area of the neuronal membrane, and it is believed that this extensive morphology gives the neuron powerful dynamic signal processing capabilities (e.g. Rall and Segev, 1987) which are not represented by highly abstract models such as the perceptron (Rosenblatt, 1962).

Dendritic Trees and Chemical Synapses

Although the electrical properties of dendrites and axons have been studied for over one hundred years, much of what is known about electrical signal spread in dendrites has been developed during the last thirty years by Wilfrid Rall and his co-workers (e.g. Rall, 1957; 1989). In this section, we limit the brief discussion to passive dendrites and refer the interested reader to (Llinas and Sugimori, 1980; Koch et al., 1983; Shepherd et al., 1989; Hounsgaard and Midtgaard, 1988) for more information on the active properties of dendrites.

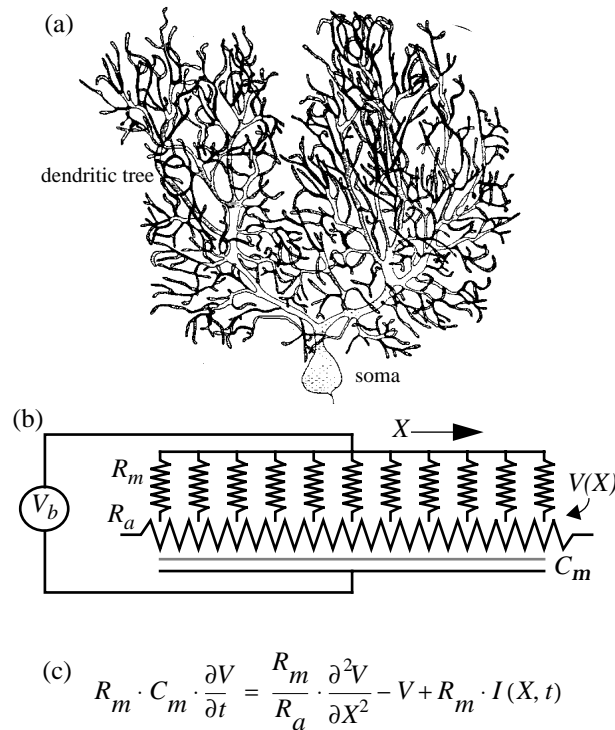


FIGURE 1. a) Drawing of typical Purkinje cell (after Berry and Bradley, 1976) from cerebellum showing extensive dendritic tree which supports $\sim 10^5$ synapses in humans. b) Electrical model for a section of passive dendrite with a membrane capacitance, C_m , in parallel with a membrane resistance, R_m , and with a series axial cytoplasmic resistance, R_a . The resting membrane voltage is determined by voltage source, V_b . c) One-dimensional cable equation which gives the membrane voltage, V , at location X at time t as a result of current density, $I(X, t)$.

It is common practice in neural network research to model the neuron as a point entity that receives and processes inputs at the soma (cell body). However, most neurons have a spatially extensive dendritic tree structure, which not only forms most of the cell's surface area but provides a spatiotemporal signal processing capability not present in traditional neural network models. Figure 1a depicts a drawing of a Purkinje neuron (Berry and Bradley, 1976) from the cerebellum which attempts to show the extensive dendritic tree structure that is common with these types of cells. The dendritic tree receives most of the afferent impulses, which in human Purkinje cells is at approximately 10^5 different synaptic locations.

Figure 1b is an electrical model for a section of passive dendrite with a membrane capacitance, C_m , in parallel with a membrane resistance, R_m , and a series axial cytoplasmic resistance, R_a . A linear second-order differential equation, the cable equation shown in figure 1c, describes the one-dimensional voltage profile for a given current density, $I(x, t)$. Transmembrane dendrite current (outward or inward) results in a soma voltage that depends in a nonlinear way on the location of the transmembrane current on the dendrite (Rall, 1964). This characteristic provides a means to scale or weight an input signal, over a wide dynamic range, by simply selecting the position for inward or outward current on the dendritic branches. The means to produce inward or outward current at particular sites is provided by the chemical synapse.

The synapse is the basic computational element of the nervous system. It is the site of signal transduction, where afferent signals, which originate from either distant or adjacent neurons, are received and combined to effect a new neuronal state. The extent of the state change is dependent on a large number of factors, not least of which is the past state trajectory. There is much experimental evidence that suggests that certain levels of afferent activity density leads to potentiation or depression of the cell's normal resting voltage that persists over widely varying times (e.g. Andersen, 1987; Hebb, 1949). These short and long term potentiation effects are thought to play an important role in neurocomputation and memory. There are at least three types of synapses in nature: chemical, electrical, and ephaptic (e.g. McCormick, 1990). In this chapter, we will focus only on emulating the computationally important behavior of the chemical synapse, which is believed to be, by far, the most common type.

We shall assume that the chemical synapse can be modeled as an ensemble of opened or closed charge-passing channels that open transiently due to the arrival of neurotransmitter at receptor sites on the postsynaptic terminal (e.g. Nicoll, 1988). If the released transmitter molecules are short lived and arrive and bind to receptor sites on the postsynaptic terminal in a time that is short compared to the postsynaptic membrane response then this process can be modeled as an impulsive event. The impulse response then depends only on the dynamics of the postsynaptic cell. If the postsynaptic cell has an Nth-order low pass filter characteristic behavior, where N is greater than unity, then its impulse response closely resembles the alpha function (Rall, 1967).

The nature of the interaction of synapses with respect to the electrical distance between simultaneously active sites is a critically important property of passive dendritic trees. An active synapse is defined as the transient opening of ion-specific channels that permits current to flow if a potential difference exists across the membrane for those specific ions. For active synapses that are temporally coincident and that are located at electrically nearby sites (i.e. the resistance between them is relatively small), the resultant signal is a sublinear function (e.g. Koch et al., 1983; Shepherd and Koch, 1990b) Conversely, for temporally coincident signals in which the active synaptic sites are electrically distant from each other, the resultant signal is nearly linear. This phenomenon is extremely important in providing a rich environment for computation.

An excitatory synapse results in a positive or depolarizing voltage trajectory if its reversal potential is greater than the membrane resting voltage. An inhibitory synapse results in a negative or hyperpolarizing voltage trajectory if its reversal potential is less than the membrane resting voltage. An important class of inhibitory synapses have their reversal potential near the normal membrane resting potential and therefore produce no voltage transitions whenever the membrane voltage is near rest. These silent synapses are believed to play a critical role in visual processing (e.g. Torre and Poggio, 1978).

The transient response of dendrites to depolarizing or hyperpolarizing synaptic activation shows two important features. First, the peak voltage amplitude as measured at the soma is largest for active sites nearest the soma and gets progressively smaller for sites further away. Second, the time at which the peak occurs shows a similar dependency on the distance from the active site so that distal sites are spread out in time and reach their peak values later than more proximal sites. This transient behavior suggests the possibility of powerful dynamic signal processing capabilities using simple circuit elements modeled after dendritic trees and chemical synapses.

Somata and Axons

The electrical response due to synaptic stimulation diffuses or propagates through the dendritic tree to all other portions of the cell interior. As the electrical signal spreads to other parts of the cell, an action potential or impulse might be generated at specialized sites along the dendrites, axons, or soma. An action potential is a highly nonlinear voltage transition that is usually triggered by the cell membrane voltage exceeding some threshold value. As mentioned previously, information is often conveyed from neuron to neuron by modulating the interpulse interval and their phase relationships. The interpulse interval can vary over a large range. Some neurons produce high pulse density bursts with long intervals in between bursts. Other neurons are continuously producing pulses with a particular interpulse interval. Synaptic activity in the dendritic tree along with cell morphology and membrane electrical properties have a dominant role in determining the resulting pulse behavior. In general, depolarizing excitatory responses tend to reduce the interpulse interval, and hyperpolarizing inhibitory responses tend to increase the interpulse interval. Silent synapses tend to play a localized inhibitory role in particular regions of the dendritic branches (e.g. Northmore and Elias, 1993).

Axons carry information in the form of encoded impulses to distant neurons. Axons are described by the same electrical model as passive dendrites and therefore are fairly lossy. In order to transmit pulses over long distances, axons often have an additional coating (myelin) that helps to reduce losses, and they have repeaters every few millimeters that regenerate the pulses.

ARTIFICIAL DENDRITE AND CHEMICAL SYNAPSE

In this section, we describe electronic circuits that 1) emulate the electrical behavior of passive dendritic trees and chemical synapses and 2) are simple and robust enough to ensure that networks, which ultimately need to support huge numbers of synapses, can be constructed with standard VLSI processing. Electronic analogs of active dendrite behavior (e.g. Llinas and Sugimori, 1980; Shepherd et al., 1985, 1989; Hounsgaard and Midtgaard, 1988) will not be treated in this chapter.

Artificial Dendrites

Passive artificial dendrites are formed by a series of standard compartments, where each compartment has a capacitor, C_m , that represents the membrane capacitance, a resistor, R_m , that represents the membrane resistance, and an axial resistor, R_a , that represents the cytoplasmic resistance (e.g. Rall, 1989). Figure 2a shows a section of artificial dendrite with five standard compartments that is part of a much longer branch like that shown in figure 2b.

The transient response of the artificial dendrite is of primary importance. Figure 2c shows the impulse response measured at point S due to inward impulse current at four different locations, A , B , C , and D on a passive artificial dendrite as represented in figure 2b. The location S represents the position of the soma. Therefore, the voltages measured at S are those that would affect somatic voltage-sensitive circuits and perhaps cause the generation of an efferent impulse.

As with biological passive dendrites, the peak voltage amplitude is largest for transmembrane current nearest the soma and gets rapidly smaller for sites further away. The time for the voltage to peak shows a similar behavior: time-to-peak-voltage increases with distance from S (e.g. Rall, 1989). The behavior shown in figure 2 illustrates how the concept of weight is an inherent property of the dendritic physical structure. It is clear that position along the artificial dendrite can be used to produce an effective weighting, in both time and amplitude, of afferent signals that are in the form of transient inward or outward currents.

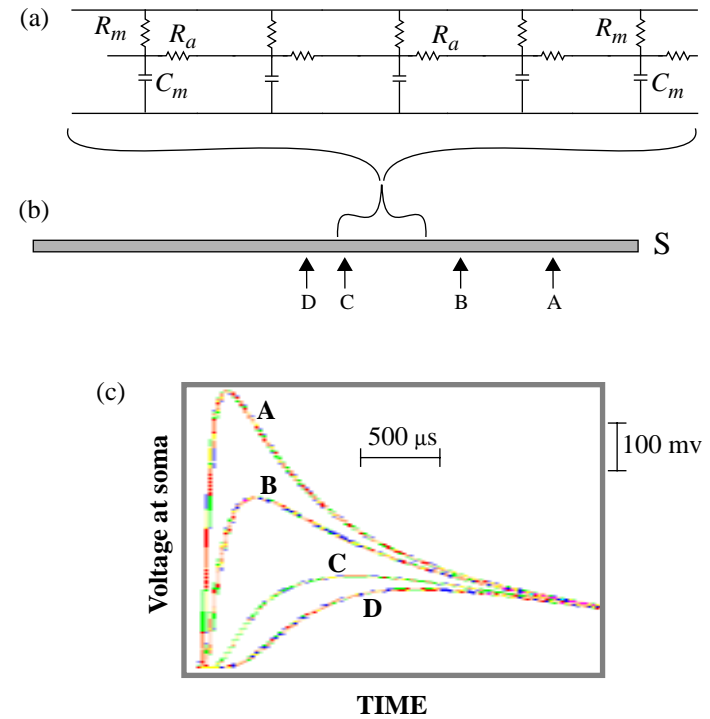


FIGURE 2. a) Compartmental model of passive dendrite. Each RC section, R_m , R_a , and C_m , is a standard compartment that simplifies VLSI layout. b) Standard compartments are abutted on substrate to form silicon dendritic branches. c) Impulse response of single artificial dendritic branch due to transient transmembrane current at indicated locations on branch.

Artificial Chemical Synapse

The means for enabling inward or outward impulsive current at a specific artificial dendrite location is accomplished by using a single MOS field effect transistor. A p-channel transistor enables inward current, which produces a depolarizing excitatory type response, and an n-channel transistor enables outward current, which results in an inhibitory type response. Some n-channel transistors have one of their terminals

connected to the resting voltage, V_{rest} , and play the role of silent or shunting inhibitory synapses. Two variants of artificial dendrites are shown in figures 3a and 3b, where p-channel (upper) and n-channel (lower) transistors are placed at uniform positions along the branch. In figure 3a, only hyperpolarizing inhibitory synapses are present, while in figure 3b, both hyperpolarizing and shunting are shown. The transistors are turned on by an impulse signal applied to their gate terminals. Both transistor types operate in the triode region. Therefore, the amount of transmembrane current depends on the conductance of the transistor in the on state, the duration of the gate terminal impulse signal, and the potential difference across the transistor, which is dependent on the state of the dendrite at the point of the synapse. All excitatory transistors have identical drawn dimensions (as do, currently, inhibitory transistors), and both excitatory and inhibitory artificial synapses are placed at the same locations in the current chip implementations. In normal operation, both excitatory and inhibitory transistors at the same site may turn on simultaneously.

Electrical Response of Artificial Dendritic Trees and Synapses

In figure 2, we illustrated the behavior of the impulse response amplitude as a function of the synapse position on the ADT, thus demonstrating the effective weighing of inputs that are mapped onto the tree structure. The impulse response amplitude as a function of the afferent impulse signal width is shown in figure 4a, which represents measured responses from one of our VLSI circuits for four different impulse widths. A similar postsynaptic behavior is found in biological preparations under presynaptic voltage-clamp: presynaptic depolarization produces a nearly linear increase in postsynaptic voltage (e.g. Angstadt and Calabrese, 1991). This behavior may be due to a lengthening of the time over which transmitter is released, thereby increasing transmembrane current in the postsynaptic terminal. In any event, the efficacy of existing connections can be changed by altering the impulse width. We are investigating how this may be done on a local basis, perhaps consistent with Hebb's postulate (Hebb, 1949), such that both local synaptic strength and the location of the synapse on the branch combine to produce an effective synaptic weight for a given connection.

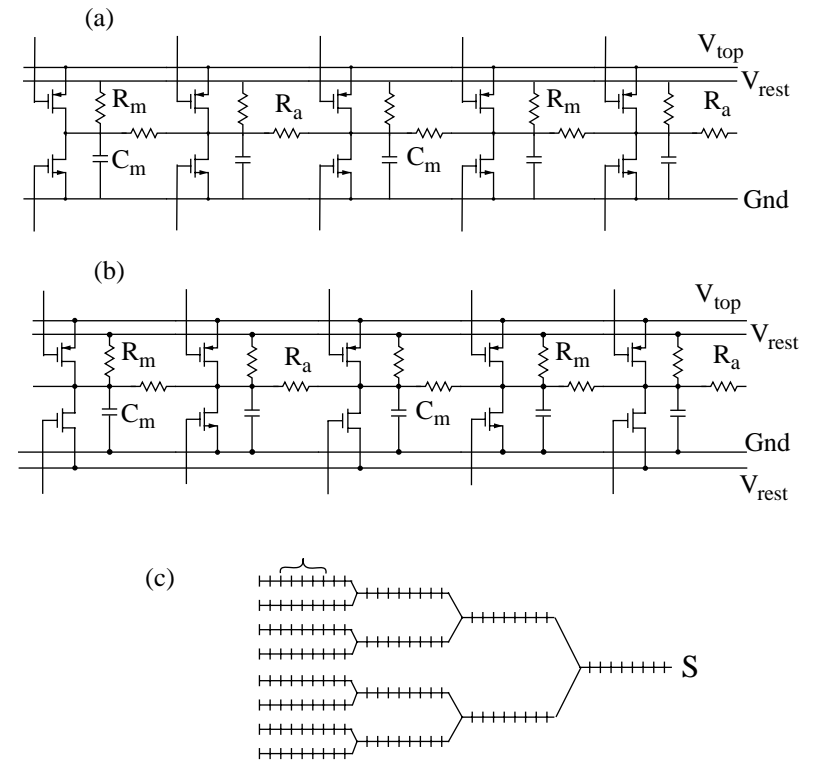


FIGURE 3. a) A five compartment section of artificial dendrite with five excitatory and five hyperpolarizing inhibitory artificial synapses. (b) Same as (a) but includes three shunting inhibitory synapses. V_{rest} is the resting voltage, V_{top} is the maximum membrane voltage. (c) A multibranched ADT which is constructed by piecing together artificial dendrite sections like that in (a) and (b).

The artificial dendrite's voltage response to closely spaced impulses is shown in figure 4b. The response due to each synaptic event is added to the resultant branch point voltage from past events until the voltage reaches a maximum value. This behavior is the expected impulse response of an Nth-order system and is solely due to the effective postsynaptic membrane. The same behavior would be observed if the phasing of multiple, transiently conducting, artificial synapses was short compared to the effective membrane constant.

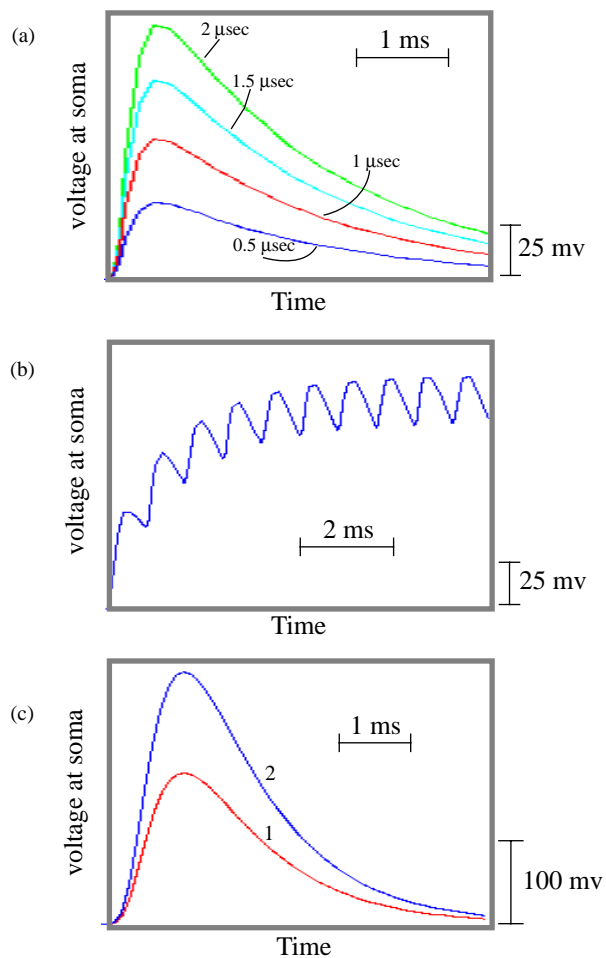


FIGURE 4. Experimental results from artificial dendrite-synapse circuit to afferent stimulation a) Graded response: amplitude of voltage peak at soma is linearly related to afferent impulse width over wide range. b) Tetanus response: closely spaced impulses cause voltage response to saturate if impulse rate is faster than membrane decay time c) Nonlinear and nearly-linear response: curve 1 is the resultant somatic voltage for simultaneous stimulation of two adjacent synapses on same branch (see fig 3c). Curve 2 is somatic voltage for simultaneous stimulation of two synapses on different branches. Positions of synapses for curves 1 and 2 were equidistant from soma.

Multiple, simultaneously conducting synapses that are electrically close together produce a voltage at the soma that is less than the sum of their individual responses (e.g. Shepherd and Koch, 1990b). This sublinear effect is due to the shunting load seen by each synaptic site when electrically nearby synapses open their channels. In contrast, multiple, simultaneously conducting synapses that are electrically far apart produce a nearly linear resultant voltage at the soma. Both of these behaviors, as measured at the trunk of a two-branched ADT (e.g. point S in figure 3c), are shown in figure 4c. The smaller voltage transient (curve 1) was measured when two adjacent artificial synapses were simultaneously active on the distal end of one of the branches. The larger voltage transient (curve 2) shows the resultant voltage when two artificial synapses on separate branches were simultaneously active. In this case, the resultant is nearly twice that of the previous example. In both cases, the artificial synapses were equal distance from the point of measurement. This type of behavior clearly enriches the signal processing capabilities of systems comprised of spatially extensive dendritic trees (Koch and Poggio, 1987).

Artificial Somata and Axons

The analog output voltage of each ADT must be processed by an impulse generating artificial soma. Although the behavior of biological somata is quite complex, and it varies considerably depending on cell type and species (e.g. Koch and Poggio, 1987), we believe a simple circuit will suffice. Soma circuits like those described by Mead (1989), Meador et. al. (1991), and Lazzaro (1992) are simple to implement and exhibit desirable behavior. We are currently investigating the use of these circuits or adaptations of them with our ADTs.

In nature, the axon is the channel over which information is conveyed to distant locations. If this was its only function we would have little need to emulate its behavior. However, axons, like dendrites, impart a delay in the flow of information, which we believe is an important system capability. Fortunately, information carried by axons is in the form of impulses which makes delaying them by arbitrary amounts of time a fairly simple matter. In our system, impulses produced by either sensors or artificial somata are captured by monitoring circuitry (see below) that can hold the impulse for a specified time before sending it to its final destination(s).

SILICON DENDRITIC TREES

If artificial dendrites are to be used in real systems then they must be implemented via a process that can make huge numbers of them in a small area inexpensively. The only feasible path for doing this currently is with standard silicon processing methods. In this section, we discuss briefly the implementation of a dendritic system in silicon. Before discussing the silicon implementation, we must say a few words about our method of making connections between synapses and impulse sources.

Convergent, Divergent, and Recurrent Connections

Networks that are built with artificial dendrites and synapses process signals that have a spatiotemporal significance by mapping afferent signal pathways to specific locations on the dendritic trees. The connections between synapses and the outputs of sensors and neurons determine the overall system response for a given dendritic dynamic behavior. The number of different connection patterns is quite large and is a factorial function of the number of synapses and sensor elements. If we limit, for the moment, the number of divergent connections to one, then the total number of different connection patterns is given by

$$\frac{N!}{(N - M)!} \quad (1)$$

where N is the number of artificial synapses and M is the number of sensor and neuron outputs. Artificial systems may have thousands of afferents and many times more synapses, resulting in an extremely large number of possible connection patterns. In our system, we allow each sensor element or artificial neuron to make unrestricted divergent connections and each synapse to receive multiple convergent connections from both sensor elements and artificial neurons. This tends to make the number of possible connection patterns much larger than that indicated by equation (1).

Virtual Wires

In the implementation of an electronic system, the number of data pathways in or out of modules is limited by the available technology. Integrated circuit packages rarely exceed 500 pins; our current artificial dendrite chips are in 40 pin packages.

This limitation in pin count is of special concern with dynamic artificial neuronal systems because of the analog nature of the computation. Each sensor or neuron output must be able to connect to any one of the artificial synapses in the system, and the spiking outputs from sensors and neurons must arrive at their artificial synapse destinations in a parallel fashion.

In order to overcome I/O limitations and to meet the connectivity and timing requirements, we make use of a multiplexing scheme that we refer to as virtual wires. In this scheme, the outputs of active neurons and sensors (i.e. those that are currently producing a spike or impulse) cause the synapses that they connect with to become activated after a delay that is specific for each efferent connection. The process of reading an active output causes that output to return to the inactive (i.e. nonspiking) state.

Virtual wires are formed using four circuits: digital or analog Stimulus Memory, which is closely associated with each synapse, Address Decoding, which serves all on-chip synapses, State Machine, which determines sensor and neuron output states, and Connection List, which specifies the locations of synapses and the axonal delay associated with each connection. Stimulus Memory and Address Decoding are on-chip circuits; the Connection List and State Machine are off-chip. With digital Stimulus Memory, the activated synapses throughout the system are turned on transiently by a global impulse stimulus signal. With analog Stimulus Memory, the synapses turn on as soon as they are activated and turn off after either a globally set or individually set delay.

The circuit diagram of a digital excitatory Stimulus Memory connected to its p-channel artificial synapse transistor is shown in figure 5. With the digital Stimulus Memory, nine transistors are needed for each artificial synapse. A synapse is activated when its `exc_syn*[n]` is set to logic 0 by asserting `SET*` while `CLEAR*` is unasserted. The `SET*` signal is asserted by the on-chip address decoder when the proper combination of external address lines and control signal are asserted. An activated synapse will turn on while the global impulse signal, `STIMULATE*`, is asserted. The global signal `CLEAR*` is asserted after every `STIMULATE*` assertion to inactivate synapses in preparation for the next round of sampling and activation.

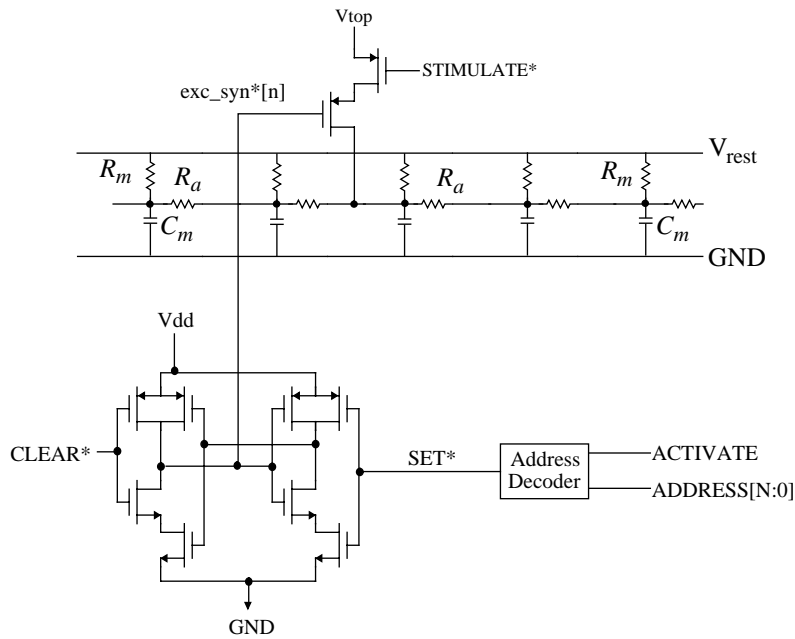


FIGURE 5. Digital excitatory Stimulus Memory shown with its p-channel synapse transistor. SET* is asserted by applying the proper address and asserting ACTIVATE. When SET* is asserted the synapse is activated (i.e. exc_syn*[n] is set to logic 0) and the artificial synapse will turn on while STIMULATE* is asserted. CLEAR* inactivates all Stimulus Memory locations throughout the system. Both STIMULATE* and CLEAR* are global signals in the system.

Digital Stimulus Memory requires a rather large number of transistors for each synapse and does not lend itself to individually variable synapse on-times as discussed above and illustrated in figure 4a. Therefore, we have designed an analog Stimulus Memory cell that is considerably simpler and provides some control over the synapse on-time. The circuit diagram of an analog inhibitory Stimulus Memory connected to its n-channel artificial synapse transistor is shown in figure 6. The same address decoder is used in both the digital and analog designs and the interface is the same except the signals CLEAR* and STIMULATE* are not required. The duration of the on-time for a particular synapse type (i.e. excitatory, hyperpolarizing, shunting) throughout a chip is controlled by separate bias voltages, V_b .

The Connection List is a multiple-bit-wide memory that holds the synapse addresses and axonal delay of each efferent connection in its domain. For large systems, we plan to divide the network into domains that will permit a certain level of parallel sampling of neuron and sensor outputs which should enhance system scalability. The Connection Lists across all domains hold the pattern of connectivity for the system and thus their contents determine system behavior. A connection pattern can be fixed in ROM, or as in our present system, loaded via computer for experimentation.

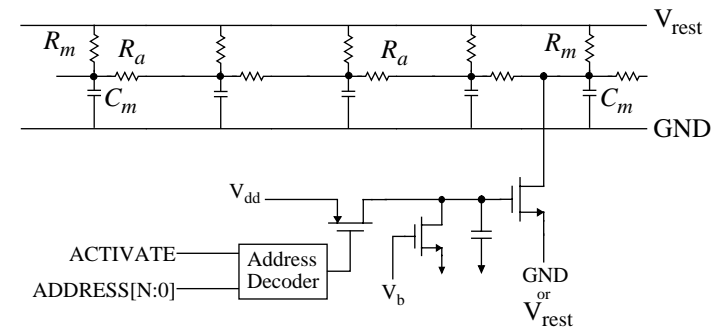


FIGURE 6. Analog inhibitory Stimulus Memory. Connection of synapse source terminal to GND results in a hyperpolarizing behavior while connection to V_{rest} produces a shunting or silent synapse behavior. The synapse turns on when a proper address is present and ACTIVATE is asserted. The on-time duration is controlled by V_b which is different for each synapse type on a chip.

Figure 7 illustrates a simplified single-domain system comprising Connection List, sensor, State Machine, and four neuromorphic chips, each of which contain a number of artificial neurons. The outputs of the artificial neurons on each chip are sampled via a multiplexer which is selected by the on-chip Address Decoder. Each neuron is in one of two states, so only a single output pin is needed to read all of them. In operation, the State Machine reads the state of each sensor element and every neuron in its domain. A spiking neuron or sensor output is detected by the State Machine which then activates all of the synapses that connect to that particular sensor or neuron. For chips with digital Stimulus Memory, STIMULATE* is asserted transiently after reading all outputs, thus turning on activated synapses while it is

asserted. This is followed by asserting $CLEAR^*$, which inactivates all synapses. For chips with analog Stimulus Memory, synapses turn as they are activated and stay on for a time that is different for each synapse type. As with Mahowald's method of connecting neuron outputs to synapses (Mahowald, 1992) addresses of synapses and neurons are used rather than direct connections carrying spikes.

Standard Dendrite Compartment

Figure 8 illustrates the basic integrated circuit layout of our standard dendrite compartment *sans* synapse transistors. Each compartment has an effective membrane capacitance, C_m , an effective membrane resistance, R_m , and an effective cytoplasmic resistance, R_a . The size of the artificial dendrite standard compartment varies with each chip design. In the past, it has ranged from $18\ \mu\text{m}$ by $180\ \mu\text{m}$ to $18\ \mu\text{m}$ by $360\ \mu\text{m}$ with most of this area being taken up by the capacitor.

The capacitor is the largest element in the standard dendrite compartment and is implemented using conventional silicon processing methods (e.g. Allen and Holberg, 1987). The capacitor was fabricated with two layers of polysilicon separated by a thin oxide layer. The top plate of the capacitor is polysilicon layer 2 (poly2) and connects to a ground bus that runs perpendicular to the long axis of the capacitor. The bottom plate is polysilicon layer 1 (poly1) which connects directly to the resistors, R_a and R_m , and to the synapse transistors in the stimulus memory (see figures 5 and 6). The capacitance varies, depending on chip design, between 1 and 2 pf, which is based on an oxide thickness of approximately $700\ \text{\AA}$. There are many techniques to reduce the footprint of the capacitor while keeping the same capacitance: thinner dielectric, use material with a higher dielectric constant, e.g. silicon nitride, employ three-dimensional capacitors, e.g. trench or tower capacitors, but we will not explore these further here.

The compartmental resistors may be implemented by a number of standard silicon fabrication techniques: well, pinched, active, and SC (e.g. Allen and Sanchez-Sinencio, 1984). The resistor footprint for a particular resistance depends not only on the resistance value but also on the implementation technique. Well resistors have a footprint advantage over the other techniques because the well resistor can be put under the capacitor. Therefore, a well resistor does not take up any silicon real estate but it has the disadvantage of relatively small resistance (measured as $5\ \text{k}\Omega$ per square for our chips). Pinched resistors have a higher resistance but can not be placed under the capacitor. Active and SC resistors require control voltages and clock signals and emulate resistor behavior over a certain range of terminal voltages and resistance values.

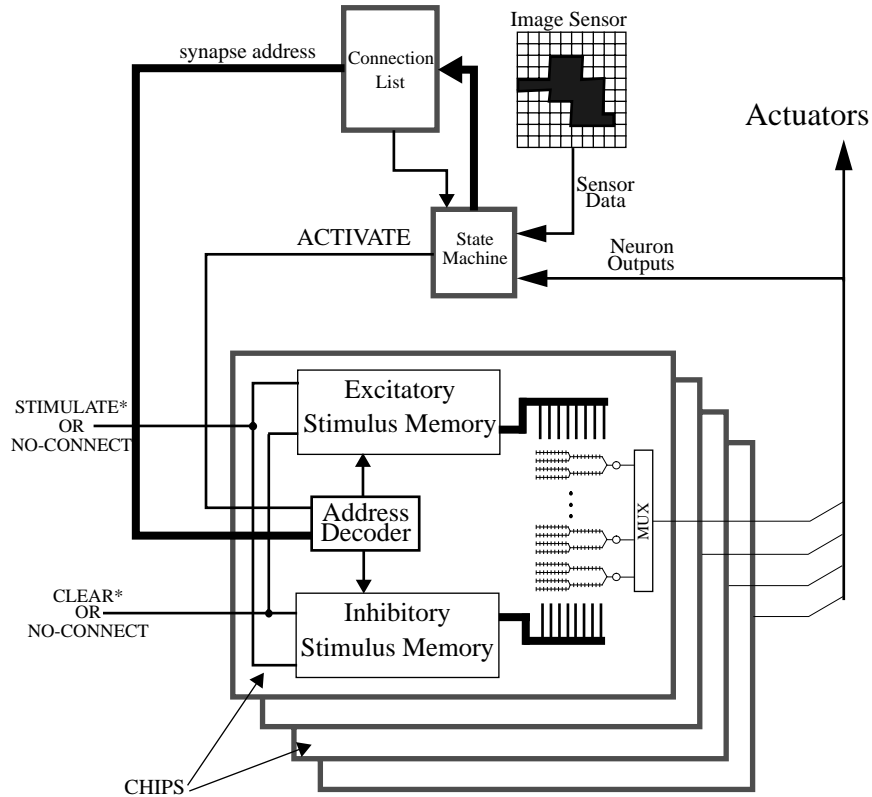


FIGURE 7. Simplified block diagram for single domain system showing basic operation. All sensory and neuronal outputs activate the artificial synapses that they connect to through the virtual wires. NO-CONNECTs are for analog Stimulus Memory implementations.

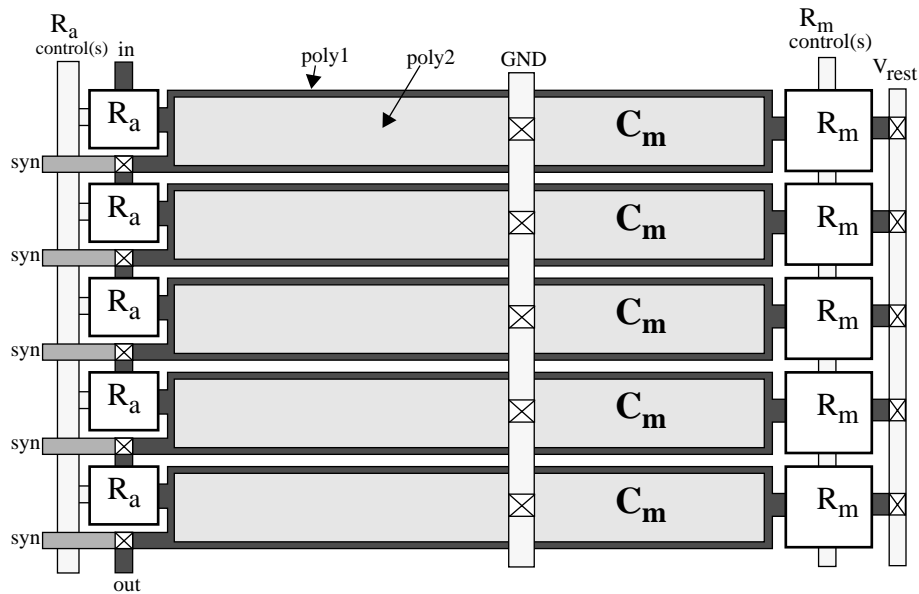


FIGURE 8. Basic VLSI layout for standard dendrite compartment. Five compartments are shown. Control lines for resistors permit adjustment of resistance over a limited range. V_{rest} establishes the resting voltage (typically 1V). The synapse transistors (not shown) connect to terminals on the left hand side labeled syn.

We have implemented n-well, active, and SC resistors on different chips and will report on the details of their design and relative behavior later (Elias and Meshreki, 1993). In our standard dendrite compartment, n-well resistors go under the capacitor and active or SC resistors are placed at the ends of the capacitor as shown in figure 8. Independent control signals for changing the resistance of the SC or active R_m and R_a pass along both sides of the compartment. For chips with active resistors, the control signals are DC voltages that permit a certain range of adjustment. With SC resistors, the control signals are AC voltages in which the frequency determines the resistance. Presently, the R_m resistors in all of the compartments share the same control signals and the R_a resistors share a different set of control signals. Therefore, all compartments have nominally the same R_m and R_a resistances.

The standard dendrite compartment was designed to abut with adjacent compartments and was pitch-matched to the on-chip virtual wire circuitry. This method makes the construction of ADTs a relatively simple task: to make a branch, standard compartments are placed side-by-side until the desired branch length is reached. Branches are then connected via metal or poly wires to form trees. The spacing between compartments is the minimum distance between capacitors ($2\ \mu\text{m}$). The compartments are aligned such that the inputs of one compartment connect to the outputs of the previous compartment.

Silicon Implementation

The ADT circuits and their on-chip virtual wiring are fabricated using a $2\ \mu\text{m}$ CMOS double-poly n-well process on a 2mm by 2mm Mosis Tiny Chip (e.g. Mead, 1989). The artificial somata and output multiplexer have been left off the chips thus far to permit experimentation with different soma circuits. Four artificial dendritic branches each having 15 excitatory and 15 hyperpolarizing inhibitory artificial synapses have been implemented on most of the chips. The number of synapses are kept low in order to leave open silicon areas on the chips for other analog test circuits.

Figure 9 shows an ADT chip layout that uses digital stimulus memory cells. In this implementation, the four branches are in-line, with a gap in between each branch, and centered on the die. The ends of each branch are taken out of the chip through package pins to allow experimentation with different tree structures. Multiple chips can be combined as well to produce tree structures with more branches, longer branches, or higher order branching. The remaining circuitry makes up the virtual wires.

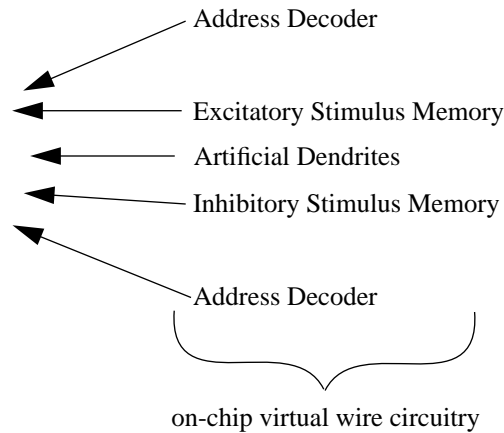


FIGURE 9. Chip layout of artificial dendrites fabricated using a MOSIS 2 μm double polysilicon standard CMOS process. The four artificial dendritic branches can be seen in the center of the die. The ends of each branch are connected to pads which allows experimentation with different branching structures. Each branch has 30 synapses (15 excitatory and 15 inhibitory) which are uniformly spaced along the branch.

TRACKING CONTROL

We are investigating the use of ADT circuits in various control and sensory processing applications. One of these makes use of ADTs to control the pointing of a video camera such that a maneuvering-target is always kept in the center of the camera's field of view. In this system, the sensor is a standard RS-170 type camera and its pointing actuators are torque motors that are antagonistic to each other. The actuators couple to the camera body via cables and cause the camera to pivot about a single point which is fixed on a multi-axis platform. Both camera and platform are controlled by similar ADT circuitry and actuators. The paired torque motors and cables are simple analogs of antagonistic muscle groups and tendons of the primate oculomotor and head systems, the camera representing an eye, and the platform

functioning as a head. In operation, the paired motors, linked by camera and platform attachment points, move against each other by applying unequal tension on the cables, thereby changing the gaze direction. In the complete system, there are two pairs of antagonistic actuators attached directly to the camera and two pairs attached to the camera's supporting platform.

Live video, directly from the camera, is displayed on a monitor, which allows observers to follow the progress of the tracking system. In operation, any target that moves into the camera's field of view will attract the system's interest and cause it to rapidly rotate the camera and platform in a direction that makes the target's image less eccentric with respect to the field of view. Rotational movement continues until the target's image is centered. The greater the target eccentricity, the greater is the peak rotational velocity of the camera.

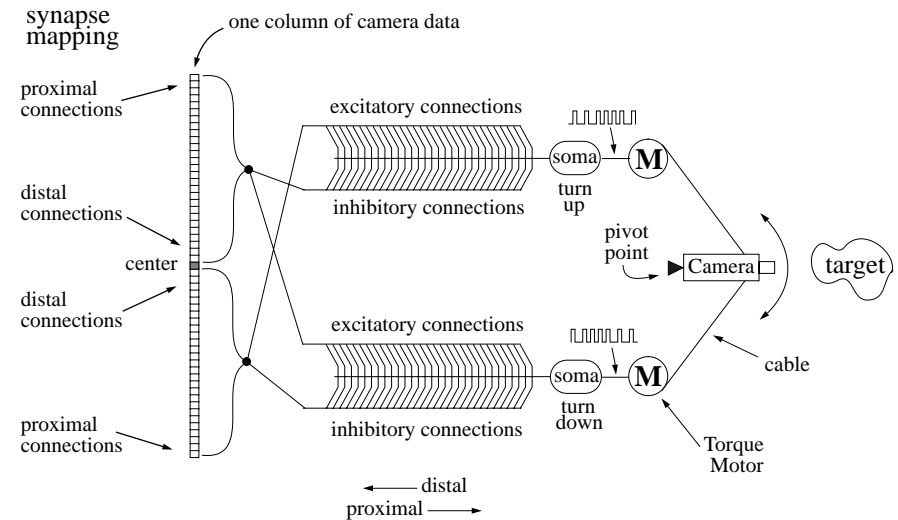


FIGURE 10. Simplified block diagram of a one-dimensional target tracking system that makes use of ADTs and oscillating artificial somata. Camera sensor elements near center make connections to distal synapses on ADTs while sensor elements near edges make connections to proximal synapses.

The one dimensional system shown in figure 10 can serve to illustrate the basic control operation of the complete system. Only two ADTs are needed for this one-dimensional target tracker. Each artificial neuron uses a single dendritic branch which has $N/2$ excitatory and $N/2$ inhibitory artificial synapses, where N is the number of sensor elements. The connections between the sensor and each artificial neuron have a simple triangular structure (Elias, 1992). However, the inhibitory and excitatory connections for each artificial neuron are mirror images of each other: the top half of the sensor makes excitatory connections to the lower ADT and inhibitory connections to the upper ADT; the bottom half of the sensor makes inhibitory connections to the lower ADT and excitatory connections to the upper. This connection pattern gives the system the ability to detect imbalance in the sensor's field of view. With an unbalanced sensor field, the outputs of the neurons are no longer of equal pulse density which forces the actuators to pull the camera in a direction that reduces the eccentricity between target and camera center.

The artificial somata are voltage controlled pulse generators which, in the absence of dendritic transients, oscillate with a center frequency of f_0 . Their output pulse streams are not synchronous and they have approximately the same center frequency, f_0 . When the target is in the center of the camera's field of view, the ADTs receive a balanced set of stimuli from the camera. Under balanced conditions, the transient output from the dendritic branch is approximately zero. Therefore, the soma center frequency remains at f_0 . When the target is off center, the dendritic branches receive an unbalanced stimulus pattern that results in a non-zero output transient. The response of the artificial somata to an excitatory input is to transiently increase the output frequency above f_0 . Presently, hyperpolarizing membrane voltage does not reduce the pulse frequency below f_0 . The amount by which f_0 changes depends on the magnitude of the integrated impulse responses from the ADT. The dynamics are dependent on the effective membrane properties and the spatial location of active artificial synapses.

In one dimension, the system operates in the following way. Assume a non-maneuvering target suddenly appears near the top of the sensor's field of view. The camera must be moved up in order to put the target's image in the center of the monitor. Due to the excitatory synaptic activity the pulse rate to the top actuator

increases which causes it to pull harder on its cable. Although there are inhibitory voltage transients on the lower ADT, the tension on the bottom stays above a minimum value. As the camera rotates towards the target, all the while reducing the eccentricity, tension on the top cable lessens until the target is centered, when once again the tension on the bottom and top cables is equal and the camera stops rotating.

As the target maneuvers away from the camera's gaze in an attempt to escape, the impulse patterns applied to the dendritic branches induce voltage transients which increase nonlinearly as the distance between target image and monitor center increases. The exact response with distance from the center depends on the actual connection pattern (Elias, 1992) between sensor elements and ADTs. A desirable connection pattern would have the controller rotate the camera faster towards the target when the distance between target image and monitor center is large compared to when the distance is small. With the target's image near the monitor center, the response is much reduced which allows a slower approach to the final camera position and a minimum amount of overshoot.

SUMMARY AND DISCUSSION

Our research program attempts to capture useful neurocomputational principles from biology by applying structure and behavior modeled after synaptic and dendritic levels of implementation. The ADT described in this chapter is the basic computational substrate in our system. Although our electronic models of chemical synapse and passive dendritic tree are, in many respects, extreme simplifications of biological structures, their dynamic electrical behavior appears to satisfactorily follow that of their biological paragons. The ADT structure is based on a current understanding of passive dendritic trees which results in an extremely simple circuit implementation that is highly scalable. Artificial neurons with extensive dendritic trees have the capability to process signals that have both temporal and spatial significance. In our networks, weights are replaced with connections which, when combined with the sublinear behavior of electrically close synapses and the nearly linear behavior of widely separated synapses, provide a rich computational substrate for signal processing.

ACKNOWLEDGMENTS

The author wishes to thank Peter Warter for several useful suggestions on chip architecture, Hsu Hua Chu and Samer Meshreki for assisting with chip layout, design, and testing.

REFERENCES

- Andersen, P.O., (1987) "Properties of hippocampal synapses of importance for integration and memory," in *Synaptic Function*, Eds. G. M. Edelman, W. E. Gall, W. M. Cowan, John Wiley & Sons, chapter 16
- Allen, P. E. and Holberg, D. R. (1987) *CMOS Analog Circuit Design*, Holt, Rinehart and Winston, New York
- Allen, P. E. and Sanchez-Sinencio, E. (1984) *Switched Capacitor Circuits*, New York, Van Nostrand Reinhold
- Angstadt, J. D. and Calabrese, R. L (1991) "Calcium Currents and Graded Synaptic Transmission between Heart Interneurons of the Leech," *J. Neuroscience*, 11(3), 746-759
- Berry, M. and Bradley, P., (1976) "The Growth of the dendritic trees of purkinje cells in the cerebellum of the rat," *Brain Res.*, 112:1-35
- Elias, J. G., (1992) "Genetic Generation of Connection Patterns for a Dynamic Artificial Neural Network," *IEEE Computer Society Press Proceedings of COGANN-92*, a workshop on combinations of genetic algorithms and neural networks
- Elias, J. G., Chu, H. H., and Meshreki, S. (1992) "A neuromorphic impulsive circuit for processing dynamic signals," *IEEE International Conference on Circuits and Systems*, vol. 5, 2208-2211
- Elias, J. G. and Meshreki, S. (1993) In preparation
- Hebb, D. O., (1949) *The Organization of Behavior*, Wiley, New York
- Hounsgaard, J. and J. Midtgaard. (1988) "Intrinsic determinants of firing pattern in Purkinje cells of the turtle cerebellum in vitro." *J. Physiol.* 402: 731-749
- Koch, C., Poggio, T., and Torre, V. (1983) "Nonlinear interactions in a dendritic tree: Localization, timing and role in information processing," *Proc. Natl. Acad. Sci.*, 80:2799-2802
- Koch, C. and Poggio, T., (1987) "Biophysics of computation: neurons, synapses and membranes," in *Synaptic Function*, Edelman, G. M., Gall, W. E., and Cowan, W. M., (eds) chap 23
- Lazzaro, J. (1992) "Low-power silicon spiking neurons and axons," *IEEE International Conference on Circuits and Systems*, vol. 5, 2220-2223
- Llinas, R. and M. Sugimori. (1980) "Electrophysical properties of in vitro purkinje cell dendrites in mammalian cerebellar slices." *J. Physiol.* 305: 197-213
- McCormick, D. A. (1990) "Membrane Properties and Neurotransmitter Actions", in *The Synaptic Organization of the Brain*, Ed. G. M. Shepherd, Oxford University Press, chapter 2
- Mahowald, M.A. (1991) "Evolving Analog VLSI Neurons," in *Single Neuron Computation*, McKenna, T., Davis, J., and Zornetzer, S. F. (eds) Academic Press, Chap 15.
- Mead, C. (1989) *Analog VLSI and Neural Systems*, Addison Wesley
- Meador, J. L., Wu, A., Cole, C., Nintunze, N., and Chintrakulchai, P. (1991) "Programmable impulse neural circuits," *IEEE Transactions on Neural Networks*, vol. 2, no. 1, 101-109
- Murray, A. F. and Smith, A. V. W., (1987) "Asynchronous arithmetic for VLSI neural systems," *Electronic Letters*, vol. 23, no. 12, 642-643
- Murray, A. F., Del Corso, D., and Tarassenko, L. (1991) "Pulse-stream VLSI neural networks mixing analog and digital techniques," *IEEE Transactions on Neural Networks*, vol. 2, no. 2, 193-204
- Nicoll, R. A. (1988) "The coupling of neurotransmitter receptors to ion channels in the brain," *Science* 241:545
- Northmore, D.P. and Elias, J. G. (1993) "Evolving networks of directionally selective artificial dendritic trees," in preparation
- Rall, W. (1957) "Membrane time constant of motoneurons," *Science* 126:454-455
- Rall, W. (1964) "Theoretical significance of dendritic trees for neuronal input-output relations," in *Neural Theory and Modeling*, R. F. Reiss, Ed., Sanford University Press, Stanford, CA., p. 73
- Rall, W. (1967) "Distinguishing theoretical synaptic potentials computed for different soma-dendritic distributions of synaptic inputs," *J. Neurophys.* 30, 1138-1168

- Rall, W. (1989) "Cable Theory for Dendritic Neurons", in *Methods in Neuronal Modeling: From Synapses to Networks*, eds. C. Koch and I. Segev, MIT Press, chapter 2
- Rall, W. and Segev, I. (1987) "Functional possibilities for synapses on dendrites and dendritic spines", in *Synaptic Function*, Eds. G. M. Edelman, W. E. Gall, W. M. Cowan, John Wiley & Sons, chapter 22
- Rapp, M., Yarom, Y., and Segev, I. (1992) "The impact of parallel fiber background activity on the cable properties of cerebellar Purkinje cells," *Neural Computation* vol. 4, 518-533
- Rosenblatt, F. (1962). *Principles of neurodynamics*. New York, Spartan
- Shepherd, G. M., Brayton, R. K., Miller, J. F., Segev, I., Rinzel, J., and Rall, W. (1985) "Signal enhancement in distal cortical dendrites by means of interactions between active dendritic spines," *Proc. Natl. Acad. Sci.* 82:2192-2195
- Shepherd, G. M., Woolf, T. B., and Carnevale, N. T.,(1989) "Comparisons between active properties of distal dendritic branches and spines: Implications for neuronal computations," *J. Cognit. Neurosci.* 1:273-286
- Shepherd, G. M. and Koch, C. (1990) "Dendritic electrotonus and synaptic integration", in *The Synaptic Organization of the Brain*, ed. G. M. Shepherd, Oxford University Press, appendix
- Shepherd, G. M. and Koch, C. (1990b) "Dendritic electrotonus and synaptic integration", in *The Synaptic Organization of the Brain*, ed. G. M. Shepherd, Oxford University Press, appendix
- Torre, V. and Poggio, T. (1978) "A synaptic mechanism possibly underlying directional selectivity to motion," *Proc. R. Soc. Lond. B.* 202, 409-416