

Switched-Capacitor Neuromorphs with Wide-Range Variable Dynamics

John G. Elias and David P. M. Northmore

University of Delaware
Newark, DE. 19716

ABSTRACT

The use of switched capacitors as wide-range, programmable resistive elements in spatially extensive artificial dendritic trees is described. We show that silicon neuromorphs with artificial dendritic trees can produce impulse responses that last millions of times longer than the initiating impulse and that dynamical responses are tunable in both shape and duration over a wide range. The switched-capacitor resistors forming a dendritic tree are shown indirectly to have a useful programmable resistance range between 500 K Ω and 1000 G Ω . Experimental results are presented that show variable impulse response functions, tunable frequency selectivity, and rate-invariance of spatiotemporal pattern responses.

INTRODUCTION

Our neuromorphs are VLSI circuits that comprise a spatially extensive artificial dendritic tree and a spike generating soma [1]. When incorporated into a network connected by a virtual wire system [1]-[3], a neuromorph's output can be transmitted over multiple pathways, each of which imparts a programmable delay to the spikes traveling on it. Figure 1a is a simplified circuit diagram of a short, five-compartment section of silicon dendrite. Each compartment has a capacitor, C_m , representing a membrane capacitance, two programmable resistors, R_m and R_a , representing a membrane resistance and a cytoplasmic resistance, and several MOS field effect transistors that simulate synapses by enabling transient inward or outward "transmembrane" current. The resulting potential appearing at the soma, point S in Figure 1b, determines the rate of

output spike firing. P-channel transistors (Fig. 1a, upper) produce excitatory effects on spike firing by increasing the membrane potential. Inhibition is mediated by two interleaved populations of n-channel transistors (Fig. 1a, lower). Half have their source terminals connected to ground and exert inhibitory effects by lowering membrane potential; the other half have their source terminals connected to a programmable voltage and exert inhibitory effects by pulling the membrane potential towards this voltage. When this voltage is set near the membrane resting voltage these transistors behave like shunting or silent inhibitory synapses [4]-[6]. For the results reported here, all of the inhibitory transistor source terminals were set to ground potential to produce only hyperpolarizing membrane potential changes.

The synapse transistors are turned on by an impulse signal applied to their gate terminals. The resultant “transmembrane” current depends on the conductance of the transistor in the on state, the duration of the gate terminal impulse signal, and the potential difference across the transistor. In most of our VLSI implementations, the dendritic branches have sixteen compartments (32 synapses) which are connected together to form artificial dendritic trees (ADTs) like that shown in Figure 1b.

Our neuromorph’s dynamics is due in large part to the Nth-order low-pass filter properties of its ADT. The spatial and temporal signal processing capabilities are indicated in Figure 1c,d by the effects of activating synapses at various positions on an ADT. The impulse responses were measured at the soma (point *S* in Figure 1b) after activating a single excitatory or inhibitory synapse at 15 different locations on an ADT. Although the synapse transistors were turned on for only 50 nsec, the resulting impulse responses last, in this case, for hundreds of milliseconds. With different dynamics, the impulse response may be made to last as long as 100 seconds or as short as 50 microseconds. The peak amplitude of the response is largest for synaptic activation nearest the soma and diminishes rapidly for sites farther away, while the latency to peak increases with distance from the soma. These effects of synapse position mimic those occurring in passive dendrites of biological neurons [7], [8]. They also illustrate how the ADT structure inherently

accords different weights to synapses: pulsatile afferent signals exert effects in time and amplitude that depend upon synapse position and the local “membrane” voltage. In this paper, we show, by using several examples, that ADT dynamics can be tuned to optimize the response for a particular signal processing goal.

VLSI IMPLEMENTATION

The dynamic behavior of our ADT-neuromorphs, like their biological counterparts [9], depends on the relative values of R_m , R_a , and C_m . The compartmental capacitor, C_m , has a fixed value between 100-1000 fF, depending on the particular chip design. Therefore, to effect changes in ADT dynamics, one requires a variable R_m , a variable R_a , or both.

Variable resistors may be realized by using MOS field effect transistors in various configurations. Three general approaches are commonly used: 1) Active [10]-[16], where the nonlinear behavior of pass transistors are linearized by the application of correction voltages to their gates. The effective resistance is controlled by a DC voltage and is largely independent of the frequency of the signals applied. 2) Switched resistor (SR), [17]-[22], where the effective resistance depends on the duty factor of the switching signal. A wide range of resistance is possible, but the effective resistance is dependent on the drain-source voltage. 3) Switched capacitor (SC), [23]-[28], where the effective resistance depends on the frequency used to switch the terminals of a capacitor. A wide range of resistance that is virtually independent of terminal voltage is realizable. With both SRs and SCs, the switching rate must be several times the maximum frequency component in the applied signal.

Figure 2a shows the circuit diagram of our standard dendrite compartment *sans* synapse circuitry and Figure 2b shows its SC implementation. Capacitor C_1 coupled with transistors M_1 and M_2 emulate the axial resistor, R_a , while C_2 , M_3 , and M_4 emulate the membrane resistor, R_m . The switches, M_1 , M_2 , M_3 , and M_4 , in the off state have a resistance of about $10^{12} \Omega$ and about 30 K Ω in the on state. The gate signals for R_a (Φ_1, Φ_2) do not overlap in the on state, ensuring that only one switch of each pair is on at a time. Similarly, the gate signals for R_m (Φ_3, Φ_4) are non-

overlapping.

Switched capacitor circuits used in filtering, amplification, or data acquisition typically use fairly large capacitances (> 10 pF) in order to reduce the effects of parallel parasitic capacitances. With ADT-neuromorphs, however, the membrane capacitance, C_m , must be considerably larger than the switched capacitances, C_1 and C_2 , in order to achieve smooth voltage transitions. Ignoring R_m , the change in C_m voltage every period, k , of switch operation is given by

$$\Delta V_{C_m} = V(R, k+1) - V(R, k) = \frac{C_1}{C_1 + C_m} \cdot (V(R, k) - V(L, k)) \quad (1)$$

where $V(R, k+1)$ and $V(R, k)$ represent the capacitor voltage at periods $k+1$ and k , respectively, and $V(L, k)$ is the left terminal voltage at period k . Minimizing C_1 and C_2 produces smoother voltage transitions and reduces the silicon real estate needed for the SCs. In our designs, C_m is small (100-1000 fF) to limit real estate usage, the still smaller values (~ 10 -100 fF) required for the switched capacitors, C_1 and C_2 , are realized with parasitic capacitances.

Seven different ADT chip designs have been fabricated and tested in our laboratory over the last 18 months. All were fabricated using a $2 \mu\text{m}$ CMOS double-poly n-well process on a 2mm by 2mm MOSIS Tiny Chip format. Figure 2c illustrates the basic integrated circuit layout of a five compartment VLSI dendrite section, excluding the synapse circuitry. In all our recent chips, the compartmental resistors, R_m and R_a , are implemented using switched capacitors.

The spike-generating soma (see Fig. 1b) is implemented as a resetting RC integrator. When the voltage across the integrating capacitor, C , exceeds a threshold voltage, V_{th} , the comparator generates a spike and discharges C . The spike is captured in a register which is sampled by virtual wire routing circuitry [1]-[3]. The spike firing frequency F_{out} is given by

$$F_{out} = -\left(RC \cdot \log\left(1 - \frac{V_{th}}{V_s}\right)\right)^{-1} \quad (2)$$

where V_s is the voltage at the soma (point S in Fig. 1b). The resistor, R , is also implemented by a switched capacitor, permitting one to tune the integration time constant.

RESULTS

Measurements were made on ADT-neuromorphs possessing various dendritic branching arrangements. Each dendritic branch had 16 excitatory and 16 inhibitory synapses. A common set of SC switching clocks (R_m_clk and R_a_clk) supplied all the branches of a neuromorph, giving each branch nominally similar dynamics. The effective resistances for R_m and R_a are given by

$$R_m = (R_m_clk \cdot C_2)^{-1} \quad R_a = (R_a_clk \cdot C_1)^{-1} \quad (3)$$

where C_1 and C_2 are the parasitic switched capacitors with capacitance of approximately 10-100 fF, R_m_clk and R_a_clk have units of Hz, and R_m and R_a have units of ohms. Two types of experiments were conducted: 1) activation of single synapses on a dendritic tree while recording voltage at the soma, and 2) activation of multiple synapses with various temporal and spatial patterns delivered by the virtual wire system while recording soma voltage and spike output. In both cases, synapses were activated by turning on the synapse transistors for 50 - 100 nsec.

Tunable Temporal Response

The variation in impulse response for small changes in dynamics is shown in Figure 3 for a four-branched neuromorph. Figure 3a shows impulse responses generated by a 50 nsec activation of a single proximal synapse when the SC clock frequencies were set near their low end to produce slow dynamics. Thus, when R_m_clk was 5 Hz, the decay time of the impulse response was nearly 20 seconds; the activation of more distal synapses produced even longer decay times (Figure 3b). The effective resistance of R_m at these low switching frequencies is over 1000 G Ω as determined by comparing experimental data to simulation results. At high switching frequency ($R_m_clk = 10$ Mhz), the decay time for the impulse response is approximately 50 μ sec.

The activation of an arbitrary set of synapses, both excitatory and inhibitory, in a temporal sequence gives rise to a complex waveform at the soma representing the summation (not necessarily linear) of individual impulse responses. The waveform shape depends on the dynamics, as shown in Figure 4 where responses to one particular sequence of synaptic

activations are plotted with Rm_clk as the parameter. Lower values of Rm_clk resulted in greater temporal summation between the impulse responses of temporally contiguous input pulses, larger excursions in membrane potential, and more spikes discharged for a given V_{th} .

Similar differences in temporal summation occur for fixed dynamics if the same pattern of synapses are activated at different temporal rates. In this case, the response waveforms exhibit very different behavior (Figures 5a-c). However, variable dynamics allows a synaptic pattern activated at different rates to generate soma voltage waveforms that are essentially identical in shape over different time scales (Figures 5d-f), analogous to wavelet dilation and contraction [29]. Figures 5d-f also shows that the output spike pattern remains constant for a given input pattern provided that soma integration time (RC in Eq. 2) is changed in proportion to ADT dynamics.

Figure 6 provides another demonstration of wide-range temporal tuning. A simulated, one-dimensional sensor array of sixteen elements was connected to synapses on an ADT-neuromorph so as to yield soma voltage waveforms that depended on the direction of target motion across the array. The synaptic connections were found by using a genetic algorithm [30] that sought to maximize the soma voltage when the target moved in one direction and minimize the voltage when the target moved in the opposite direction. As can be seen in Figure 6b, the soma voltage clearly differentiates direction of motion for a target moving at 10,000 sensor elements per second. In order to differentiate direction of movement for targets of different speeds, the same connections and neuromorph architecture can be used if the ADT dynamics are tuned appropriately for the desired target speed. This is shown in the experimental measurements of Figures 6b-f where the target speed and dynamics were changed by five orders of magnitude with only slight differences in the measured soma waveforms.

Tunable Frequency Response

In a functioning network, multiple sources of spikes provide a complex spatiotemporal pattern of input to an ADT-neuromorph, which responds by generating a new temporal pattern of output spikes. In the following examples, however, we present a highly simplified case of a single input

spike train of constant frequency that simultaneously activates a set of synapses on one neuromorph. By suitable choice of the synapses activated, and of the spike generator threshold V_{th} , the ADT-neuromorph may be made to exhibit a variety of frequency selectivities that can be tuned by varying the dendritic dynamics. In all examples, the mean spike frequency of the output was measured in the steady state i.e., 50 ms after of the start of the input train.

Figure 7 shows “high-pass” responses obtained by activating a set of eight distal excitatory synapses on a two-branched tree under different dendritic dynamics. Spike output cut-off frequency is a linear function of the switched-capacitor frequency. Figure 8 shows that neuromorphs can be made to exhibit a frequency band selectivity when the input spike train activates an appropriate combination of both excitatory and inhibitory synapses. The position of the peak band-selective response depends on ADT dynamics and is linearly dependent on SC switching rate over the entire range. Spike generator threshold, V_{th} , which strongly affects the shape of the band-selective function, was adjusted at each SC clock frequency to bring the peak output firing rate to approximately the same level.

SUMMARY

Switched capacitors represent a promising method of implementing wide-range programmable resistors in our artificial dendritic trees. The achievable resistance is 500 K Ω to 1000 G Ω , a range of six orders of magnitude. Our SC circuits require little silicon real estate, with only two minimum-size transistors needed for each resistor, and they provide a way to match neuromorph dynamical response with application dynamics by simply changing SC clock frequency either on a chip or a neuromorph basis. The advantage is that a single chip design can be used repetitively in a system, with each chip independently programmed to produce appropriate dynamical behavior for the particular application.

ACKNOWLEDGEMENTS

This work was supported by grants from the National Science Foundation (# BCS-9315879) and the University of Delaware Research Foundation.

REFERENCES

- [1] J. G. Elias, "Artificial Dendritic Trees," *Neural Computation* vol. 5, pp. 648-664, 1993.
- [2] J. G. Elias, H. Chu, and S. M. Meshreki, "A neuromorphic impulsive circuit for processing dynamic signals," *Proc. Int. Sym. Circuits and Systems*, 5, 2208-2211, 1992.
- [3] J. G. Elias, "Silicon dendritic trees," in *Silicon Implementation of Pulse-Coded Neural Networks*, eds. M. E. Zaghoul, J. Meador, and R. W. Newcomb, Chap 3, 1994.
- [4] V. Torre and T. Poggio, "A synaptic mechanism possibly underlying directional selectivity to motion," *Proc. R. Soc. Lond. B.* vol 202, pp. 409-416, 1978.
- [5] C. Koch and T. Poggio, "Biophysics of computation: neurons, synapses, and membranes," In *Synaptic Function* edited by G.M. Edelman, W.E. Gall, W.M. Cowan. Wiley-Liss, New York, pp. 637-697, 1987.
- [6] C. Koch, T. Poggio, and V. Torre, "Nonlinear interactions in a dendritic tree: Localization, timing and role in information processing," *Proc. Natl. Acad. Sci.* vol. 80 pp. 2799-2802.
- [7] W. Rall, "Theoretical significance of dendritic trees for neuronal input-output relations," in *Neural Theory and Modeling*, R. F. Reiss, Ed., Stanford University Press, pp. 73-79, 1964.
- [8] G. M. Shepherd and C. Koch, "Dendritic electrotonus and synaptic integration", in *The Synaptic Organization of the Brain*, ed. G. M. Shepherd, Oxford University Press, appendix, 1990.
- [9] W. Rall, "Cable properties of dendrites and effect of synaptic location," in *Excitatory Synaptic Mechanisms*, P. Andersen and J. K. S. Jansen, eds. Universitetsforlaget, Oslo, 1970.
- [10] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Holt, Rinehart and Winston, New York, 1987.
- [11] C. Mead, *Analog VLSI and Neural Systems*, Addison Wesley, 1989.
- [12] M. Banu and Y. Tsividis, "Floating voltage-controlled resistors in CMOS technology," *Electronics Letters*, vol. 18, no. 15, pp. 678-679, 1982.
- [13] K. Nagaraj, "New CMOS floating voltage-controlled resistor," *Electron. Lett.*, vol. 22, pp. 667-668, 1986.
- [14] S. P. Singh, J. V. Hanson, and J. Vlach, "A New Floating Resistor for CMOS Technology," *IEEE Trans. Circuits Systems*, vol. 36, no. 9, pp. 1217-1220, 1989.
- [15] M. Steyaert, J. Silva-Martinez, and W. Sansen, "High frequency saturated CMOS floating resistor for full-differential analog signal processors", *Electron. Lett.*, vol. 27, pp. 1609-1611, 1991.
- [16] S. Sakurai and M. Ismail, "A CMOS square-law programmable floating resistor independent of the threshold voltage", *IEEE Trans. Circuits Systems II*, vol. 39, pp. 565-574, 1992.

- [17] P. M. Embree, "The analysis and performance of a tunable state variable filter employing switched resistor elements," in *Proc. Int. Symp. Circuits Systems*, 1983, pp. 857-860.
- [18] S. E. Rehan and M. I. Elmasry, "VLSI implementation of a prototype MLP using novel programmable switched-resistor CMOS ANN chip," in *Proc. World Congress Neural Networks*, 1993, vol. IV, pp. 95-98.
- [19] S. Y. Foo, L. R. Anderson, and Y. Takefuji, "Analog components for the VLSI of neural networks," *IEEE Circuits Dev. Mag.*, vol. 6, no. 4, pp. 18-26, 1990.
- [20] S. Fukai, M. Tsukahara, and H. Ishikawa, "Realization of grounded/ungrounded and equal/unequal-valued switched-resistors," *Electronics Comm. Japan Part 1*, vol. 71, no. 5, pp. 6-14, 1988.
- [21] R. L. Geiger, P. E. Allen, and D. T. Ngo, "Switched-resistor filters---a continuous time approach to monolithic MOS filter design," *IEEE Trans. Circuits Systems*, vol. 29, no. 5, pp. 306-315, 1982.
- [22] S. E. Rehan, "Design considerations for switched-resistor active filters," M. Sc. Thesis, Mansoura University, Egypt, 1987.
- [23] P. E. Allen and E. Sanchez-Sinencio, *Switched Capacitor Circuits*. New York: Van Nostrand Reinhold Company, 1984.
- [24] A. Rodriguez-Vazquez, R. Dominguez-Castro, A. Rueda, J. L. Huertas, and E. Sanchez-Sinencio, "Nonlinear switched-capacitor 'neural' networks for optimization problems," *IEEE Trans. on Circuits Syst.*, vol. 37, no. 3, pp. 384-398, 1990.
- [25] B. J. Maundy and E. I. Elmasry, "A self-organizing switched-capacitor neural network," *IEEE Trans. on Circuits Syst.*, vol. 38, no. 12, pp. 1556-1563, 1991.
- [26] Y. P. Tsividis and D. Anastassiou, "Switched capacitor neural networks," *Electronics Letters*, vol. 23, no. 18, pp. 958-959, 1987.
- [27] A. Rodriguez-Vazquez, A. Rueda, J. L. Huertas, and R. Dominguez-Castro, "Switched-capacitor neural networks for linear programming," *Electronics Letters*, vol. 24, no. 8, pp. 496-497, 1988.
- [28] Y. He and U. Cilingiroglu, "A charge-based on-chip adaptation Kohonen neural network," *IEEE Trans. Neural Networks*, vol. 4, no. 3, pp. 462-469, 1993.
- [29] I. Daubechies, *Ten Lectures on Wavelets*. Capital City Press, Montpelier, Vermont, 1992.
- [30] J. G. Elias, "Genetic Generation of Connection Patterns for a Dynamic Artificial Neural Network," in *COGANN-92, Combinations of Genetic Algorithms and Neural Networks*, eds. L. D. Whitley and J. D. Schaffer, IEEE Computer Society Press, Los Alamitos, CA, pp. 38-54, 1992.

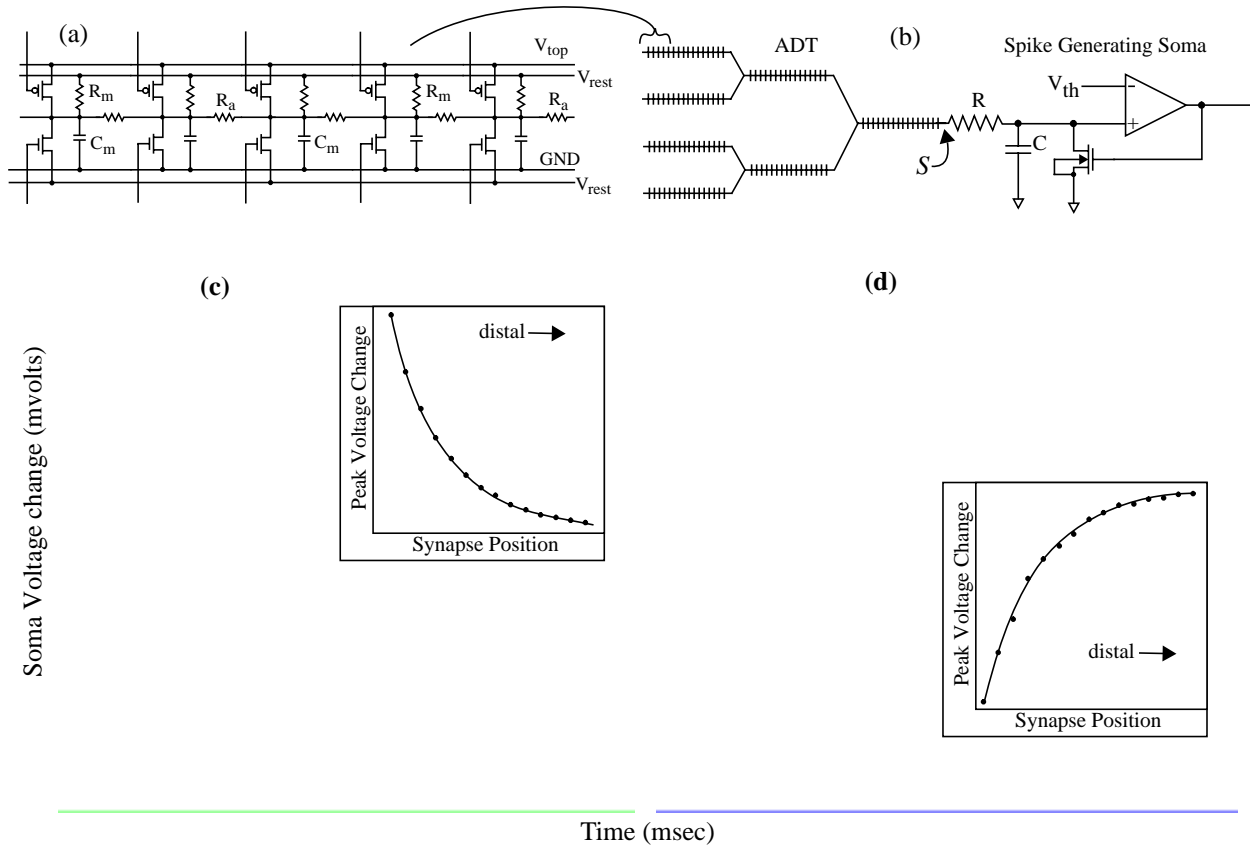


FIGURE 1. a) Five compartment segment of artificial dendrite. b) Diagram of VLSI neuromorph comprising a spatially extensive artificial dendritic tree (ADT), a spike generating soma, and a programmable number of spike output pathways that connect to synapses on ADTs. Each pathway has independent programmable delay. The crosses on the ADT represent synapse locations. c) and d) Measured impulse responses at soma (point S) due to activating a single synapse at different locations for 100 nsec. Note that the response lasts over 1,000,000 times longer than the signal that caused it. Insets show the peak voltage change as a function of synapse position.

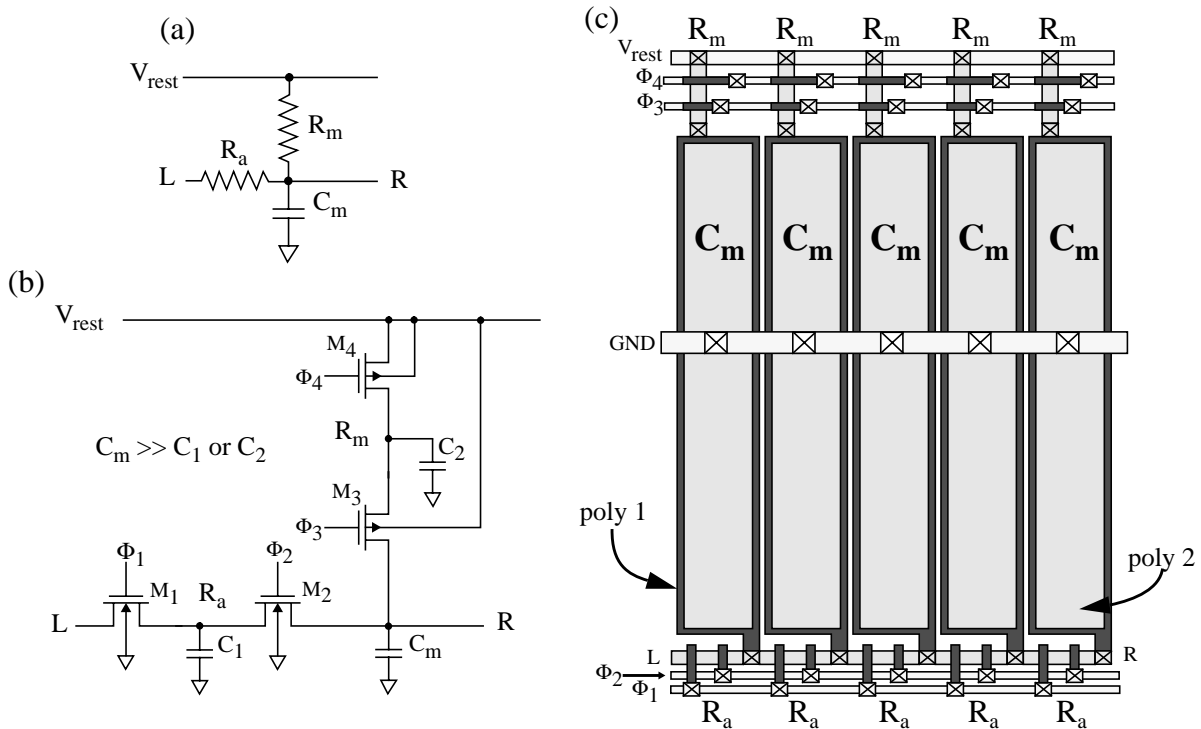


FIGURE 1. a) Circuit diagram of basic ADT compartment *sans* synapse circuitry. b) Switched capacitor implementation of compartmental resistances. Transistors M_3 , M_4 and capacitor C_2 emulate R_m . Transistors M_1 , M_2 , and capacitor C_1 emulate R_a . Clocks, ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 , permit adjustment of resistance by changing frequency according to Eqs. 3. V_{rest} establishes the resting voltage (typically 2.5V). c) Basic VLSI layout. Five compartments are abutted together to form a short dendrite branch section (synapse circuitry not shown). The compartmental capacitor, C_m , is implemented with poly1/poly2 plates and varies between 0.1-1.0 pF, depending on the particular chip design. Construction of ADTs is done by placing compartments side-by-side until the desired branch length is reached. Branches are then connected via metal or poly wires to form trees. The spacing between compartments is 2 μm , and they are aligned such that the inputs of one compartment connect to the outputs of the previous compartment.

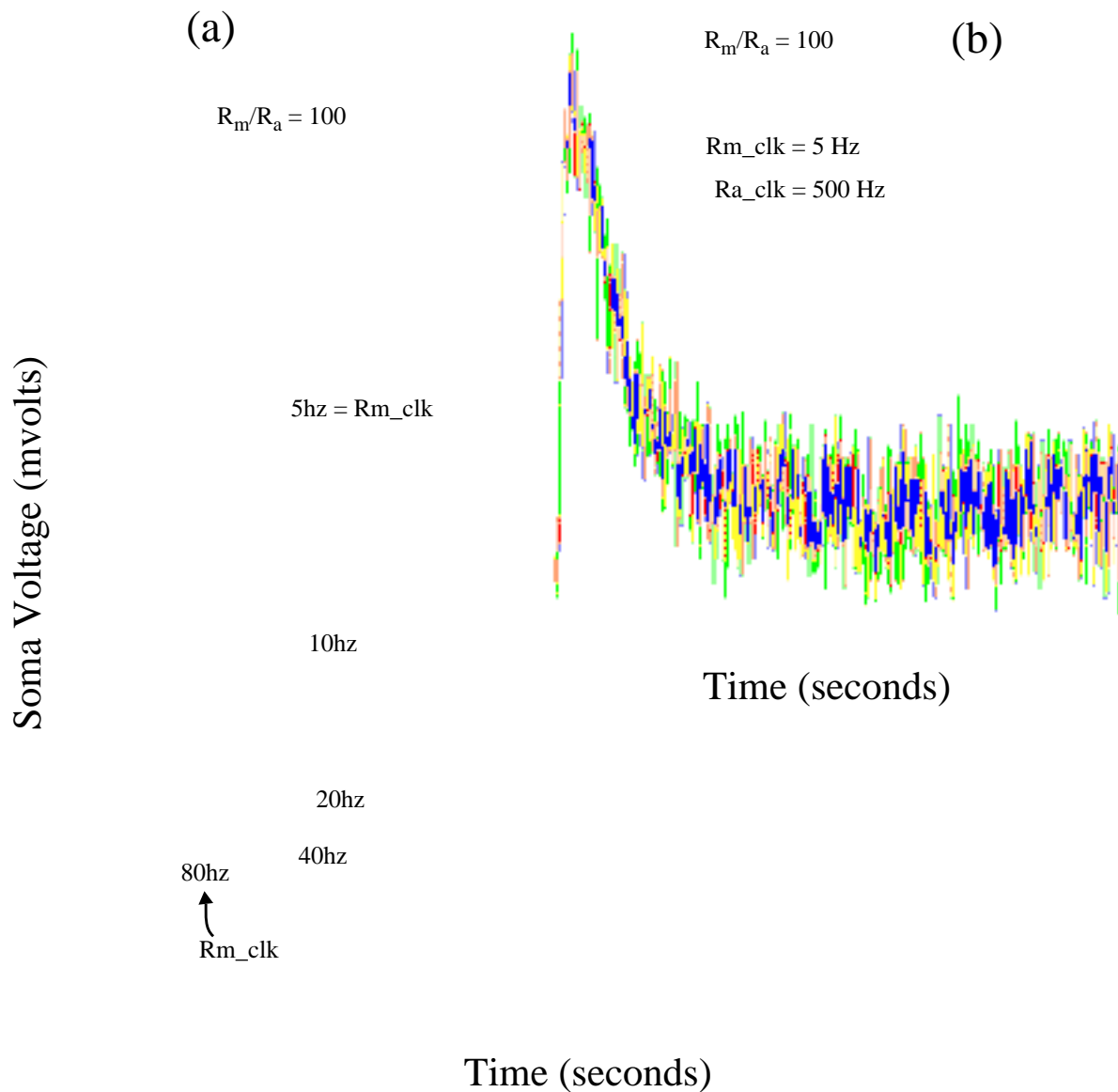
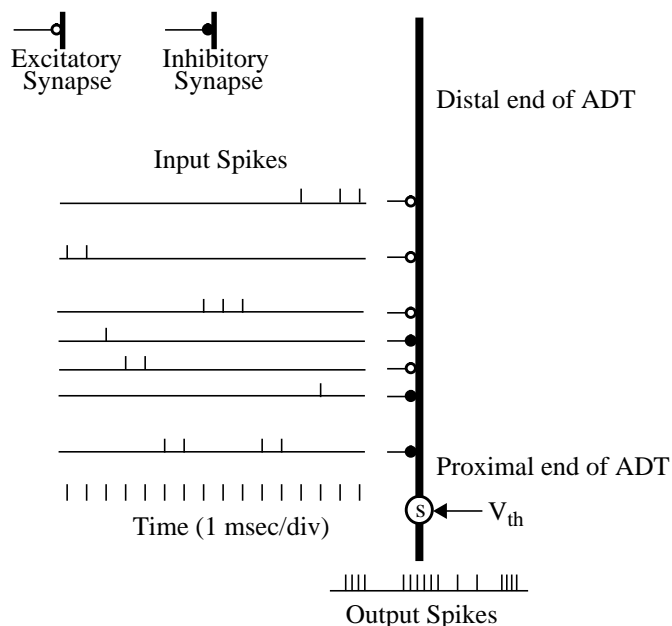


FIGURE 1. Impulse response due to activating a single synapse for 50 nsec. In these experiments, the switched capacitor clock frequencies were set near their low end to produce very slow dynamics. At the lowest setting, where R_m_clk was 5 Hz, the decay time was nearly 20 seconds. In each recording, the frequency of R_a_clk was 100 times that of R_m_clk . Activating more distal synapses using these dynamics produce even longer decay times. The effective R_m resistance at the low end of switching frequency is over $1000 \text{ G}\Omega$ a) proximal synapse (i.e., near soma) b) midbranch synapse

(a)



(b)

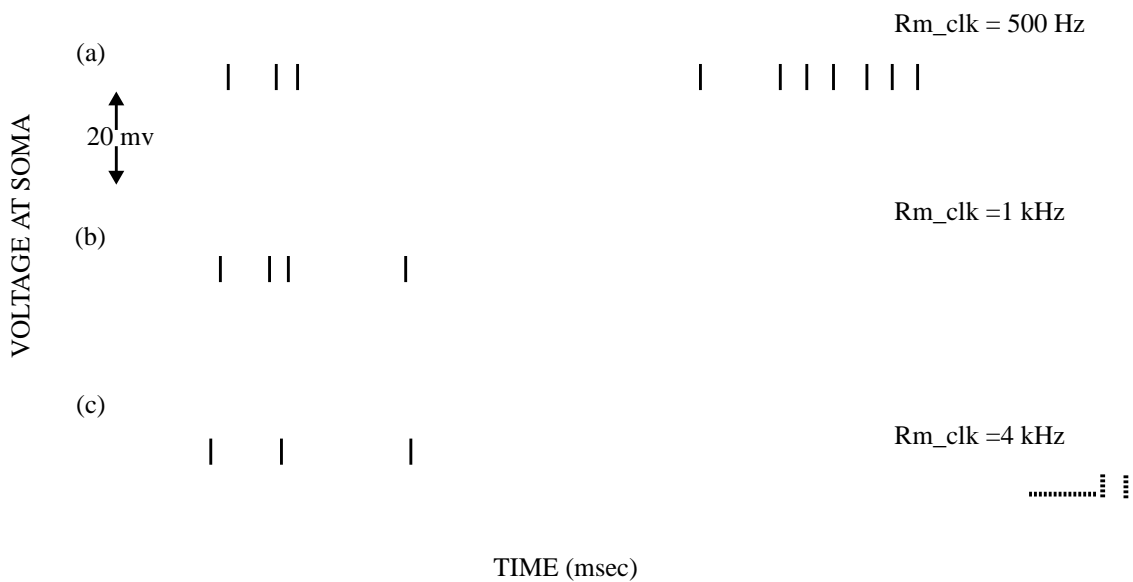


FIGURE 1. An arbitrary spatial and temporal pattern of sixteen input spikes separated by 1 msec was applied to the synapses of an ADT-neuromorph as shown in (a). At the same time, the soma voltage and output spiking pattern were measured for three different settings of ADT dynamics, shown at right end of waveforms in (b). In all cases, $R_m/R_a = 100$; $V_{th} = 2.60$ volts; spike generator RC = 2.2 msec. Output spikes are shown under their corresponding waveforms.

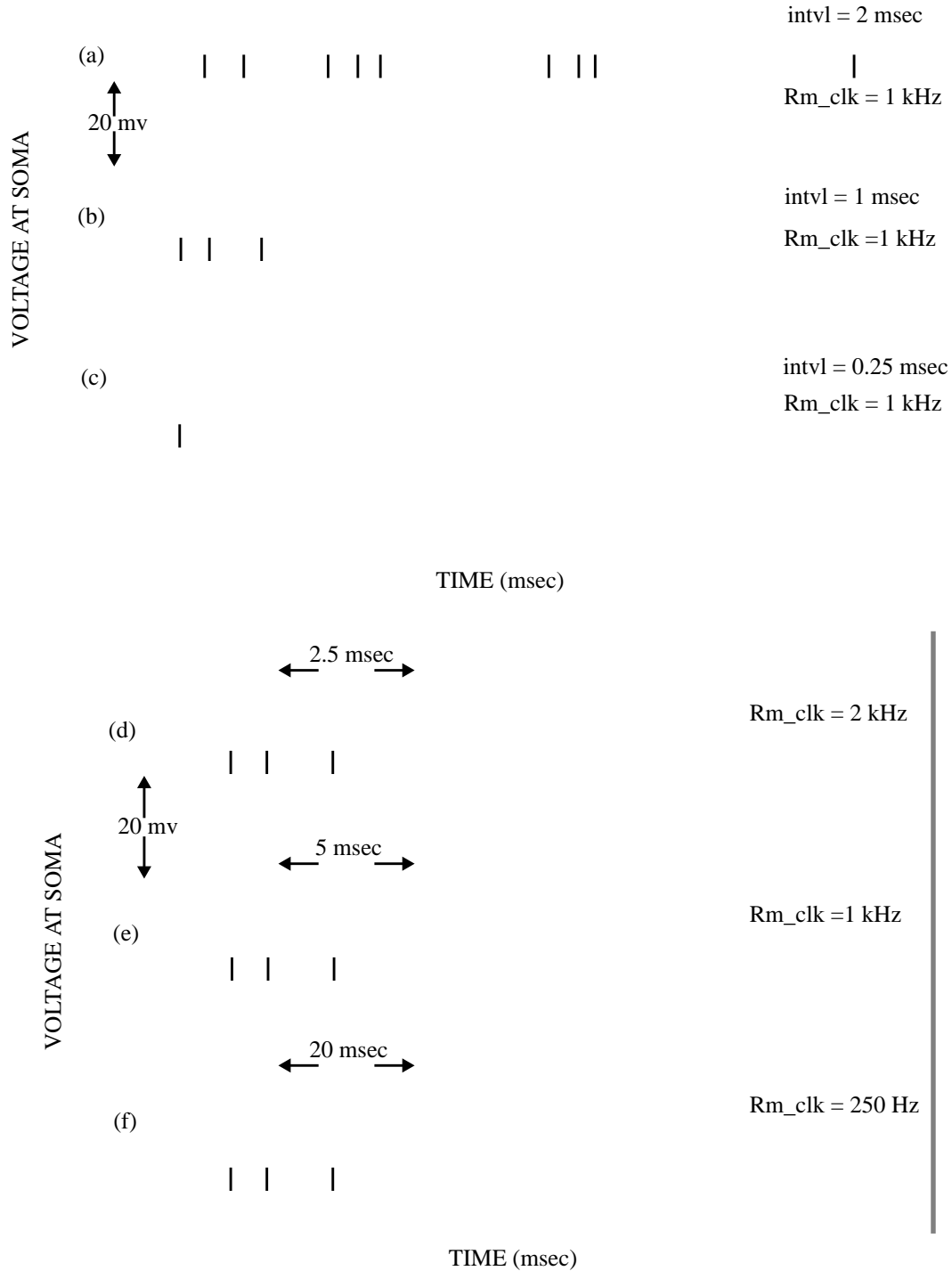


FIGURE 1. Effects of varying synapse activation interval (intvl) on soma voltage and spike output. The same spatial pattern of synapses as used in fig.4 were activated at a) 2.0 msec, b) 1.0 msec, and c) 0.25 msec intervals, with fixed ADT dynamics ($R_m/R_a = 100$; $Rm_clk = 1$ KHz). Spike generator $RC = 2.2$ msec. Changing Rm_clk in proportion to the rate of synapse activation generates equivalent soma waveforms but on different time scales, d) 2.5 msec/div, e) 5.0 msec/div, and f) 20 msec/div. The spike generator RC was also changed in proportion to Rm_clk , giving equivalent patterns of output spikes. Output spikes are shown under their corresponding waveforms.

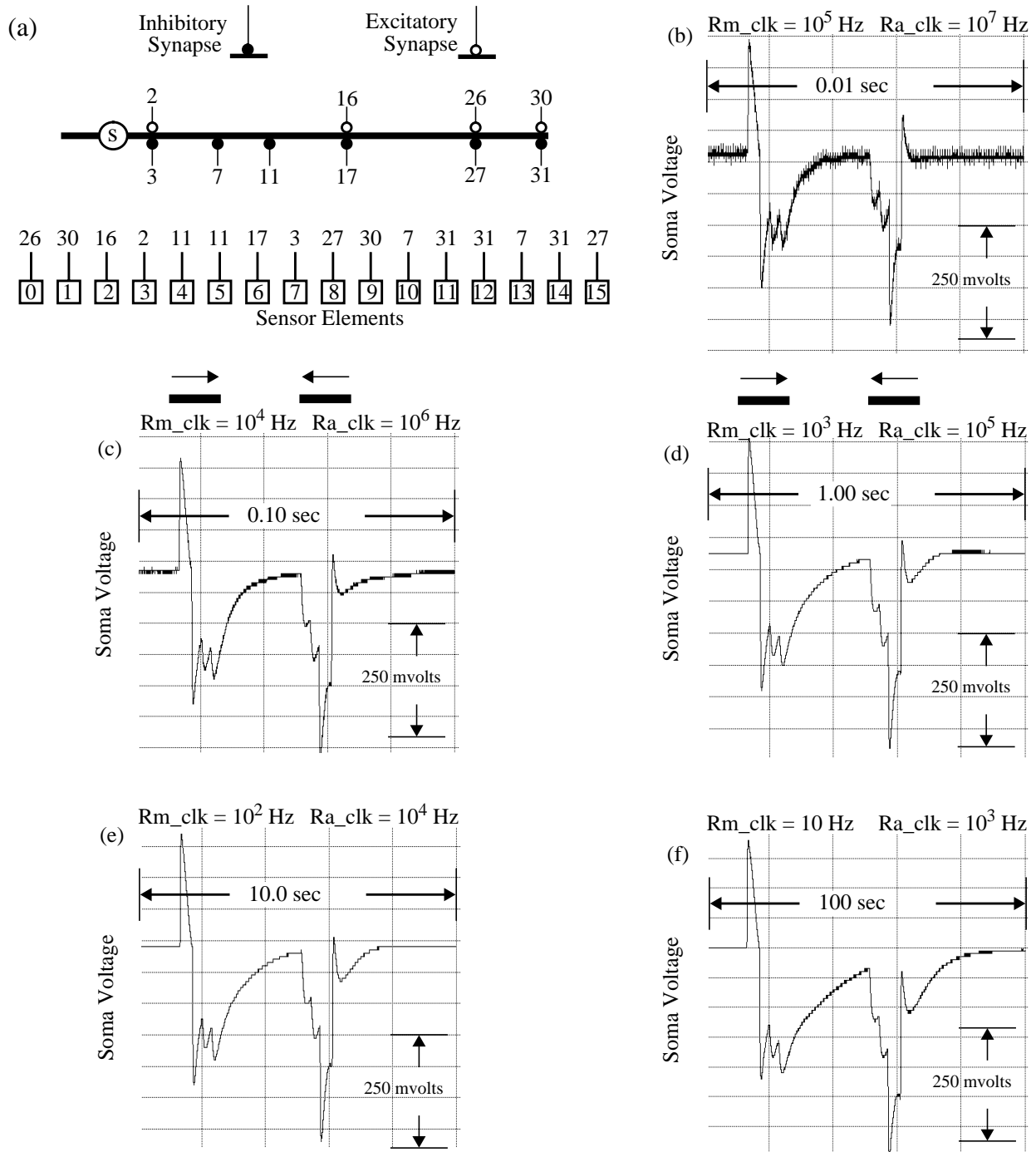


FIGURE 1. Soma voltage evoked by a point target moving to and fro across a simulated sensor array. Sixteen sensor elements were connected to synapses on an ADT-neuromorph as shown in (a). A point target traversed the array first in one direction and later in the opposite direction. Bars above figures indicate time over which target is in motion and its direction. The recordings were obtained at five different target speeds spanning five orders of magnitude. ADT dynamics were set proportionately to speed. Nothing was changed between the recordings except for target speed and neuromorph dynamics. Target speed: b) 10,000 sensors/sec. c) 1000 sensors/sec. d) 100 sensors/sec. e) 10 sensors/sec. f) 1 sensor/sec.

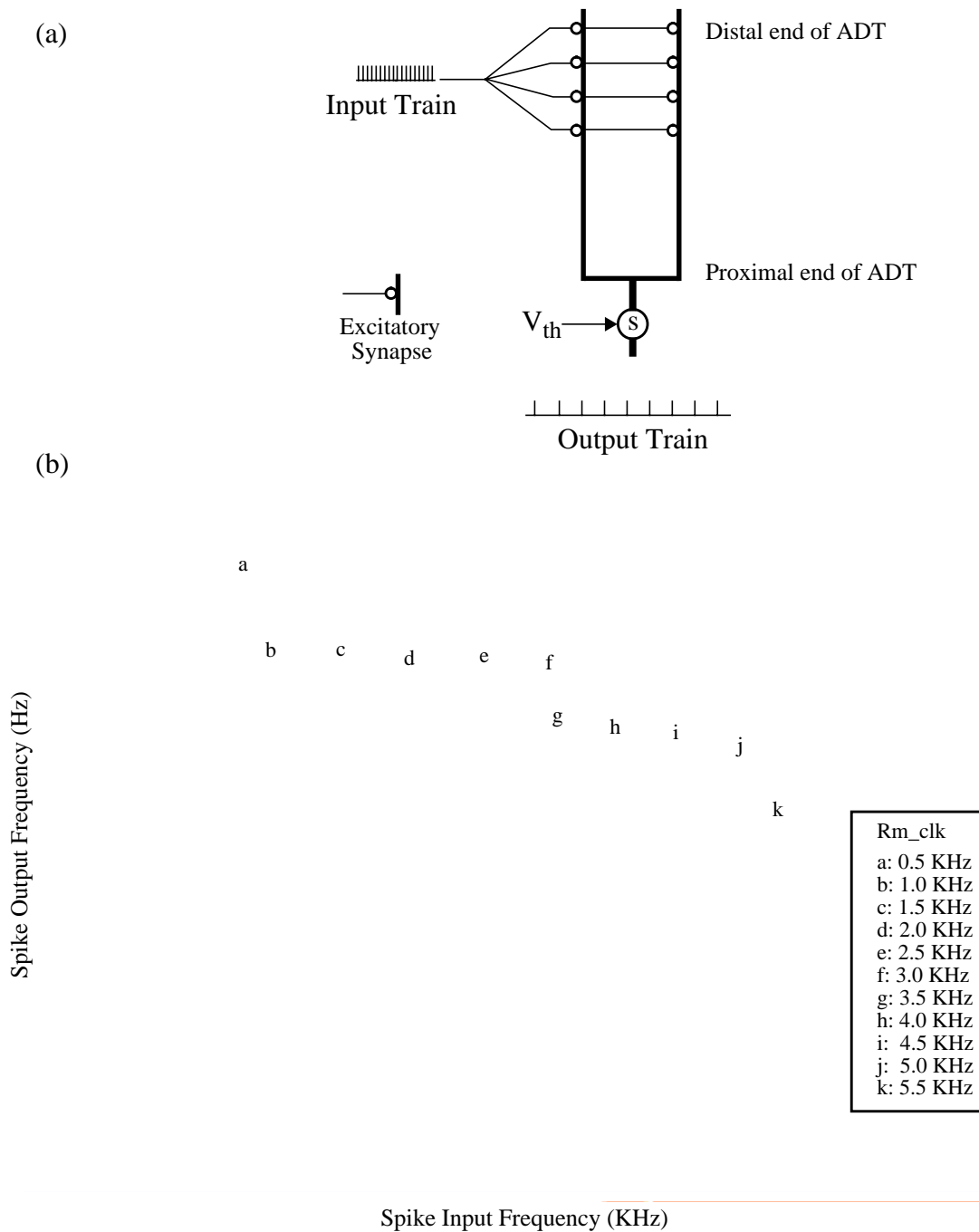


FIGURE 1. Effect of varying dynamics on “high-pass” input-output spike frequency functions for an ADT-neuromorph with two dendritic branches. a) Each spike of a constant frequency input train simultaneously activated four excitatory synapses at the distal end of each dendritic branch. Output spike frequency was obtained by averaging the spike intervals in the steady state. b) Cut-off frequency increased linearly with increasing frequency of Rm_clk . In all cases, Ra_clk frequency = $100 * Rm_clk$. Spike generator threshold, $V_{th} = 2.65$ volts.

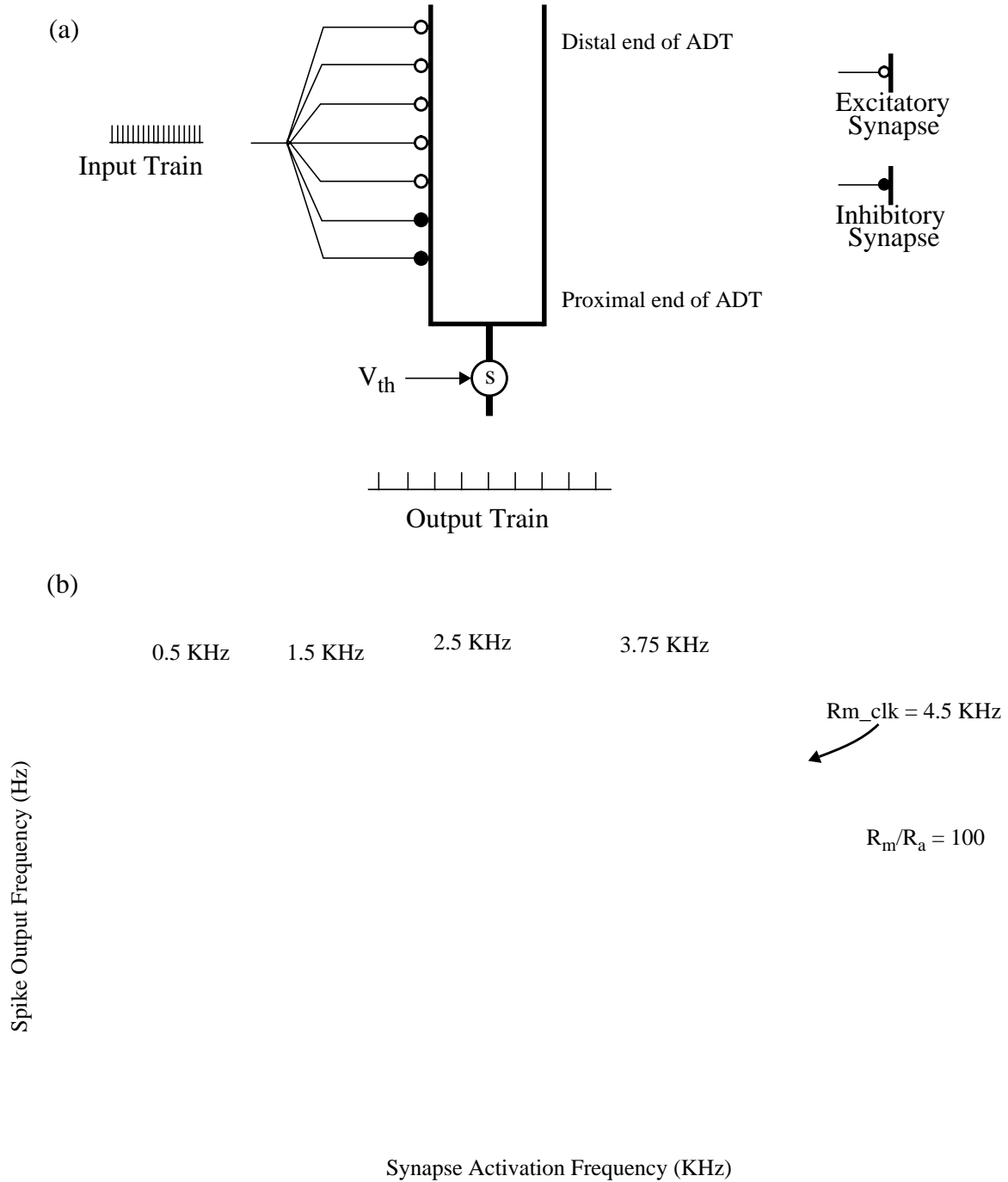


FIGURE 1. Effect of varying dynamics on “band-selective” input-output spike frequency functions for an ADT-neuromorph with two dendritic branches. a) Each input spike simultaneously activated 5 excitatory and 2 inhibitory synapses in the middle of one dendritic branch. Output spike frequency was measured as in Fig. 7. V_{th} was adjusted to equalize the peak output firing frequencies. b) Results with five different values of R_{m_clk} are shown, in all cases $R_{a_clk} = 100 \cdot R_{m_clk}$. The location of the peak frequency increased linearly with switching frequency.