THE UNIVERSITY OF MICHIGAN

Memorandum 13

SYSTEM/360 INTERFACE ENGINEERING REPORT

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PREFACE

The System/360 interface provides a connection be-
tween the PDP-8 and the multiplexor channel of System/360 models
30, 40, and 50, as well as the 2870 Multiplexor Channel attached
to other models. Either byte-interleaved or burst-mode opera-
tion can be sustained at transmission rates up to 70 kilobytes-
per-second. Interface control operations are supervised via
the PDP-8 accumulator and interrupt facilities, while data
transfer operations are directed via the three-cycle data break
facility. The interface is attached directly to the channel-
control unit interface cables which interconnect the IBM equip-
ment and occupies one control unit position on the channel.
The equipment satisfies all original equipment manufacturer's
(OEM) specifications as described in the following IBM publica-
tions:

1. System/360 I/O Interface: Channel to Control Unit
   Original Equipment Manufacturer's Information, IBM
   Corporation, Form A22-6843-3.

2. System/360 Power Control Interface: Original Equip-
   ment Manufacturer's Information, IBM Corporation,
   Form A22-6906-0.

The accompanying photographs on the next two pages
show the Data Concentrator, including the System/360 interface
together with its test panel. The interface itself is as-
sembled in the bays immediately above the test panel.

Figure i. The Data Concentrator. The Interface is in the Bay immediately above the Test Panel.
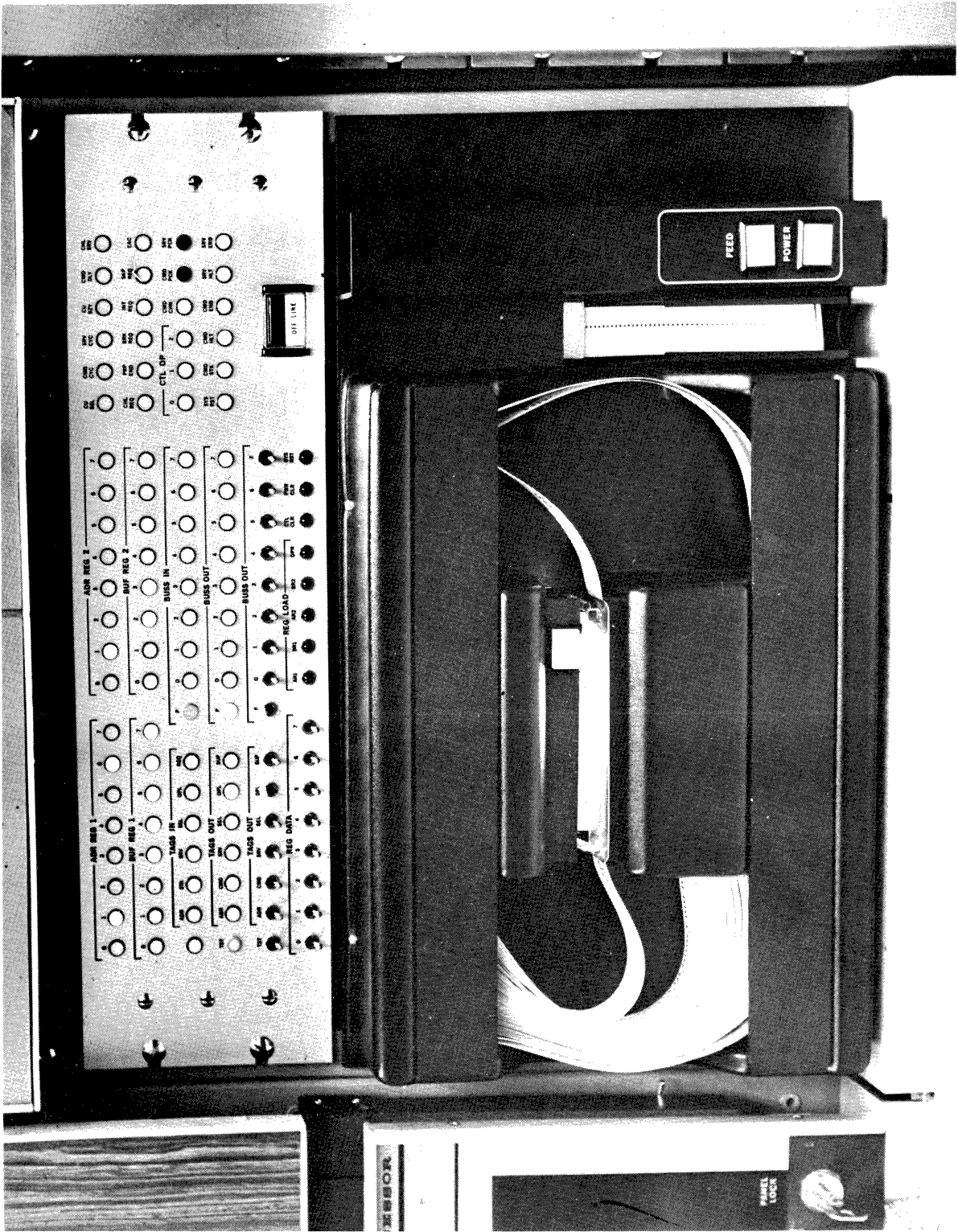
Figure ii. The Test Panel of the Interface.

ACKNOWLEDGMENTS

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SYSTEM/360 INTERFACE ENGINEERING REPORT

I. INTRODUCTION

The System/360 interface appears to the resident System/360 control program as similar to the 2702 Transmission Control. This approach is felt more fruitful in the face of heavy commitments to software support provided by the manufacturer. Its pertinent features are as follows:

a. The interface recognizes a class of device addresses that are assigned according to the conventions established by IBM.

b. Recognition of command codes and generation of status responses are in most cases under the control of the resident PDP-8 control program.

c. Several buffer registers isolate the two machines so that the exchange of control and data information does not affect the timing of other control units that may be attached to the channel.

d. Data transmission between the two machines proceeds in a byte-interleaved or burst-mode fashion at an aggregate data rate which may be programmed by the PDP-8 and indirectly by the System/360.

The System/360 interface consists of two principal components: the command interface, which services initial commands issued by the System/360 control program through the multiplexor channel, and the service interface, which transmits data and status information between the two machines. Both of these interfaces operate independently and in an overlapped fashion except at the channel interface circuitry itself, which is necessarily sequential in operation. At the channel interface the entire PDP-8 system appears to the System/360 as a control unit and accesses the interface transmission lines in the fashion prescribed for these devices.

II. CHANNEL INTERFACE LINES

The System/360 interface is connected to the multi-plexor channel via a set of 34 lines which are common to all other control units serviced by the channel. All of these lines except one are simply looped through the interface and attached to the various bus drivers or receivers as required. Thus in off-line or power-down situations it is not necessary to physically reroute or switch these lines, but merely to gate off the bus drivers and receivers. The one exception (the SEL OUT line) is physically broken at the interface. The interface-inbound SEL OUT line is routed to a terminator and bus receiver, while the interface-outbound SEL OUT line is routed from a bus driver. During normal equipment operation, signals received on the inbound SEL OUT line are processed internally and then propagated to the next control unit via the outbound SEL OUT line. During off-line or power-down conditions the terminator, bus receiver, and driver are bypassed with a relay.

The interface lines and their nomenclature used throughout this document are summarized in Figure 1. Following is a brief description of the function of each of these lines. For greater detail, the reader is referred to the pertinent IBM publications.

BUS OUT. A set of nine lines, including a parity line, which propagates outbound information a byte at a time from the channel to all control units serviced by the channel. The information is conditioned by the outbound tag lines (ADR OUT, CMD OUT, SRV OUT) actuated by the channel and may represent a device address, a control unit command, or an outbound data byte.

BUS IN. A set of nine lines, including a parity line, which propagates inbound information a byte at a time from a selected control unit to the channel. The information

BUS OUT

CHANNEL   BUS IN   CONTROL UNIT

ADR OUT
CMD OUT   OUTBOUND TAGS
SRV OUT

ADR IN
STA IN   INBOUND TAGS
SRV IN

SEL OUT
SEL IN
OPL OUT
OPL IN   SELECTION
HLD OUT   CONTROLS
SUP OUT
REQ IN

MTR OUT*
MTR IN*   METERING
CLK OUT*   CONTROLS

*NOT USED
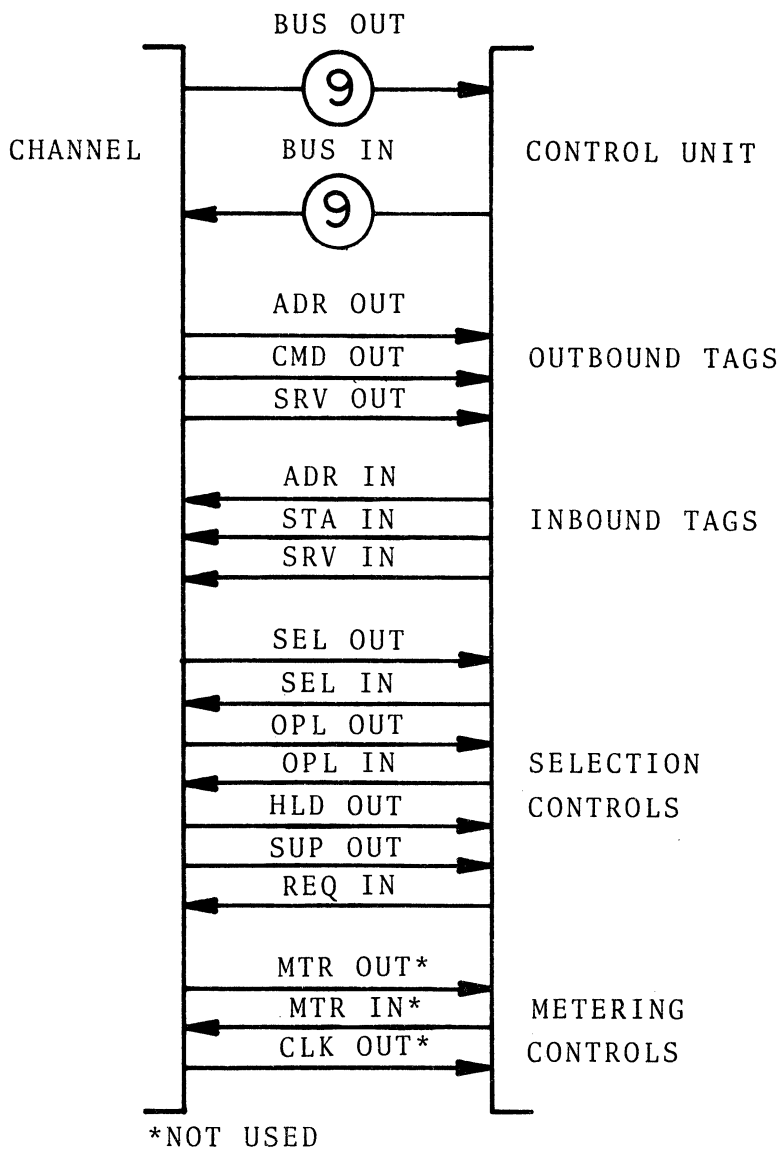
FIUGRE 1. CHANNEL-CONTROL UNIT INTERFACE LINES

is conditioned by the inbound tag lines (ADR IN, STA IN, SRV IN) actuated by the control unit and may represent a device address, a status byte, or an inbound data byte.

Outbound Tags. Three lines: ADR OUT, CMD OUT, and SRV OUT used to condition information on BUS OUT. If ADR OUT is up, the channel is attempting to gain initial selection of a control unit in order to transmit a command byte. When selection is achieved, CMD OUT indicates that a command byte is available on BUS OUT for interpretation by the control unit. SRV OUT is used as an interlock during data and status transmission cycles. These tags are also used in combination during certain control sequences not involving the use of BUS OUT.

Inbound Tags. Three lines: ADR IN, STA IN, and SRV IN used to condition information on BUS IN. If ADR IN is raised by the control unit, the information provided on BUS IN identifies the particular device requesting channel service. If STA IN is raised by the control unit, the information on BUS IN is the status byte pertaining to the device, and if SRV IN is raised, the control unit is requesting channel service for a data byte.

Selection Controls. Seven lines controlling the seizure and sequencing of transmission operations between the channel and the control unit. SEL OUT and SEL IN form a loop from the channel outbound through all control units in turn and finally inbound to the channel. A signal propagated on this line is intercepted by a control unit depending upon its position along this loop, which in effect establishes its priority for channel service. OPL OUT and OPL IN are conditioned by the channel and the control unit respectively and indicate the availability and connection

status of each of these devices. In particular, a control
unit raises OPL IN when it has achieved selection on the
interface, and is held up for the duration of the partic-
ular channel-control unit sequence involved. HLD OUT is
used in conjunction with SEL OUT to minimize propagation
delays through the select circuitry of the control units.
SUP OUT is raised by the channel to inhibit control unit
seizure of the interface under certain conditions. REQ IN
is raised by each control unit requesting channel service
and conditions the channel to poll the interface for
seizure. Certain combinations of these selection control
lines are used to indicate special conditions such as
system and selective reset, and in conjunction with the
outbound tag lines to indicate special conditions such
as interface disconnect.

   Metering Controls. Three lines used to condition
usage meters on the various devices of a System/360 complex.
The equipment described herein makes no use of these lines.

III. CONTROL SEQUENCES

   A number of control sequences are possible between
the channel and the interface and, of these, most have several
variations. All sequences can be grouped in one of three
classes, however:

   1. those involving initial-command selection,
   2. those involving data transmission, and
   3. those involving presentation of ending status.

For any one device, these sequences proceed in the order named;
that is, the device is selected and logically connected to the
channel, then transmits its data, and finally transmits status
regarding the condition of the I/O device at the conclusion of

the operation. However, certain conditions can occur which are
asynchronous to the progression of an operation through the
states corresponding to the three principal sequences. Such
conditions include those that halt data transmission and those
that test device status during the course of an operation.
Some of these can be produced by the channel without interven-
tion by the program. The operation of the interface using
typical sequences is summarized below. Additional details of
operation in exceptional cases are discussed in the pertinent
IBM publications.

3.1 Initial Selection Sequence

Figure 2* shows the sequence of interface tag line
signals during an initial selection procedure. This sequence
is used for all channel commands and, in addition, for the Test
I/O (TIO) sequence. The sequence begins when ADR OUT is raised
by the channel while a device address is on BUS OUT. If the
address has odd parity and lies within the block recognized by
a control unit, that control unit prepares to seize the channel
when SEL OUT rises on the interface. When this occurs, the
control unit

a. inhibits propagation of SEL OUT to the next lower-
priority control unit on the interface,

b. raises OPL IN to indicate to the channel that the
control unit has in fact seized the interface, and

c. internally stores the device address presented on
BUS OUT.

The channel then acknowledges OPL IN by dropping ADR OUT. The
control unit then places the just-stored device address on BUS
IN with odd parity and raises ADR IN. This returned address
is checked by the channel for correct parity and for match

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* Wave forms shown in bottom of figures correspond to inter-
face circuitry signals described in Section V. Timing in-
formation is given in the form of channel sequence photo-
graphs in Appendix B.
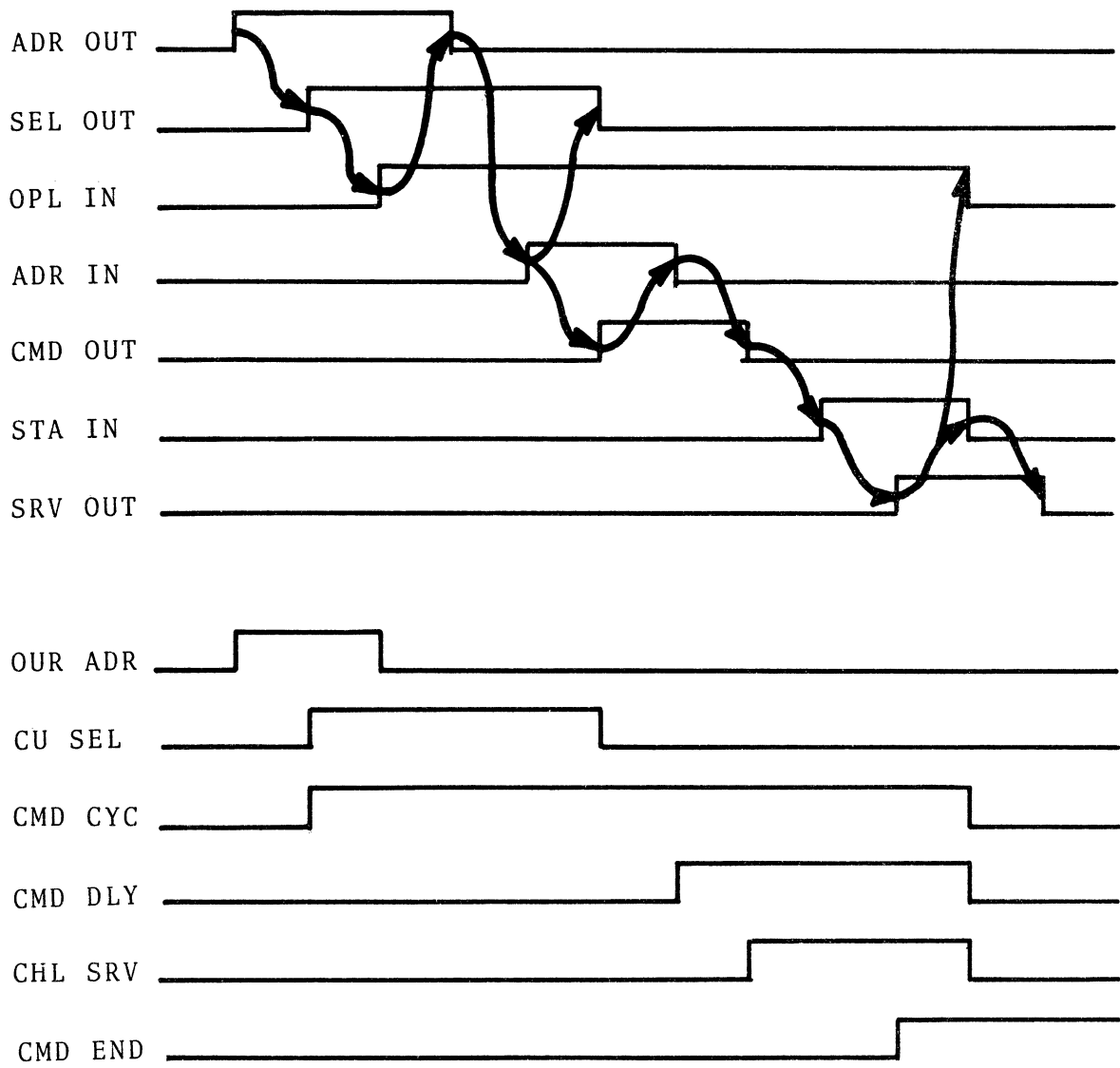
FIGURE 2. INITIAL SELECTION

against the address first transmitted on BUS OUT. If these
tests fail, the channel performs a malfunction reset, which
affects all I/O devices attached to the channel. Depending
upon the particular machine model, this operation may result
in a processor check or in a bit set in the Channel Status
Word (CSW) stored as the result of the channel operation.

Following reception of a correct address on BUS IN,
the channel next places the command byte (all zero bits for
a TIO, nonzero for a valid channel command) on BUS OUT, and
raises CMD OUT. The control unit stores the channel command
internally and checks the byte for odd parity. Following this
operation, the control unit drops ADR IN, which the channel
acknowledges by dropping CMD OUT, an invitation for the control
unit to present a status byte.

In most IBM control units, the allowable channel
commands are well prescribed and represent only a few of the
possible 255 codes. Accordingly, it is possible to detect
immediately upon storage of the channel command byte whether
the control unit can accept the particular command or not.
Thus the control unit has the option of either accepting the
command by presenting the channel with an all-zero status byte
or rejecting the command with a status byte containing the unit
check bit. In the equipment described here, the command may
undergo analysis by the PDP-8 program, a process which may
require a lengthy period compared to the channel selection
sequence. Accordingly any channel command, other than TIO,
is always accepted, even if it does not have odd parity. It
is up to the PDP-8 program to interpret the particular command
code and to transmit possible rejection using an ending-status
presentation containing the unit check bit.

Thus, following the acceptance of the channel com-
mand, the control unit places an all-zero status byte on BUS IN
and raises STA IN, to which the channel responds with SRV OUT.
The control unit now drops all inbound tag and bus lines and
disconnects from the interface. If the channel forces burst
mode at this time, SEL OUT will still be up at the control unit,

and a sequence of SRV IN-SRV OUT signals is expected by the channel to transmit the data associated with the operation. However, the multiplex channel will force burst mode only in connection with an Initial Program Load (IPL) operation. Therefore the equipment considered here is not normally expected to operate under channel-forced burst mode conditions.

3.2 Service Cycle

Figure 3 shows the sequence of interface tag line signals during a service cycle procedure. This sequence is used for all data and status byte transmission between the channel and the control unit. In the byte-interleaved mode, one such sequence is executed for each data byte separately. In the control-unit-forced burst mode, the initial part of the service cycle sequence is followed by alternate SRV IN-SRV OUT pairs.

The service cycle sequence differs from the initial selection sequence in that the transmission is initiated by the control unit rather than by the channel. A control unit requesting service raises the REQ IN tag line when the SUP OUT tag line is down at the control unit. (Certain sequences are expected to override the SUP OUT signal; see below.) When the channel next polls the control unit interface by raising SEL OUT, the highest priority control unit requesting service inhibits the propagation of SEL OUT, places its device address on BUS IN, and raises OPL IN and ADR IN. The channel checks the device address for odd parity, retrieves the addressed subchannel status in its active registers, and issues CMD OUT.

The control unit recognizes CMD OUT as permission to proceed with the operation, and it next drops ADR IN. When the channel drops CMD OUT the control unit raises either

a. STA IN and places a status byte on BUS IN,
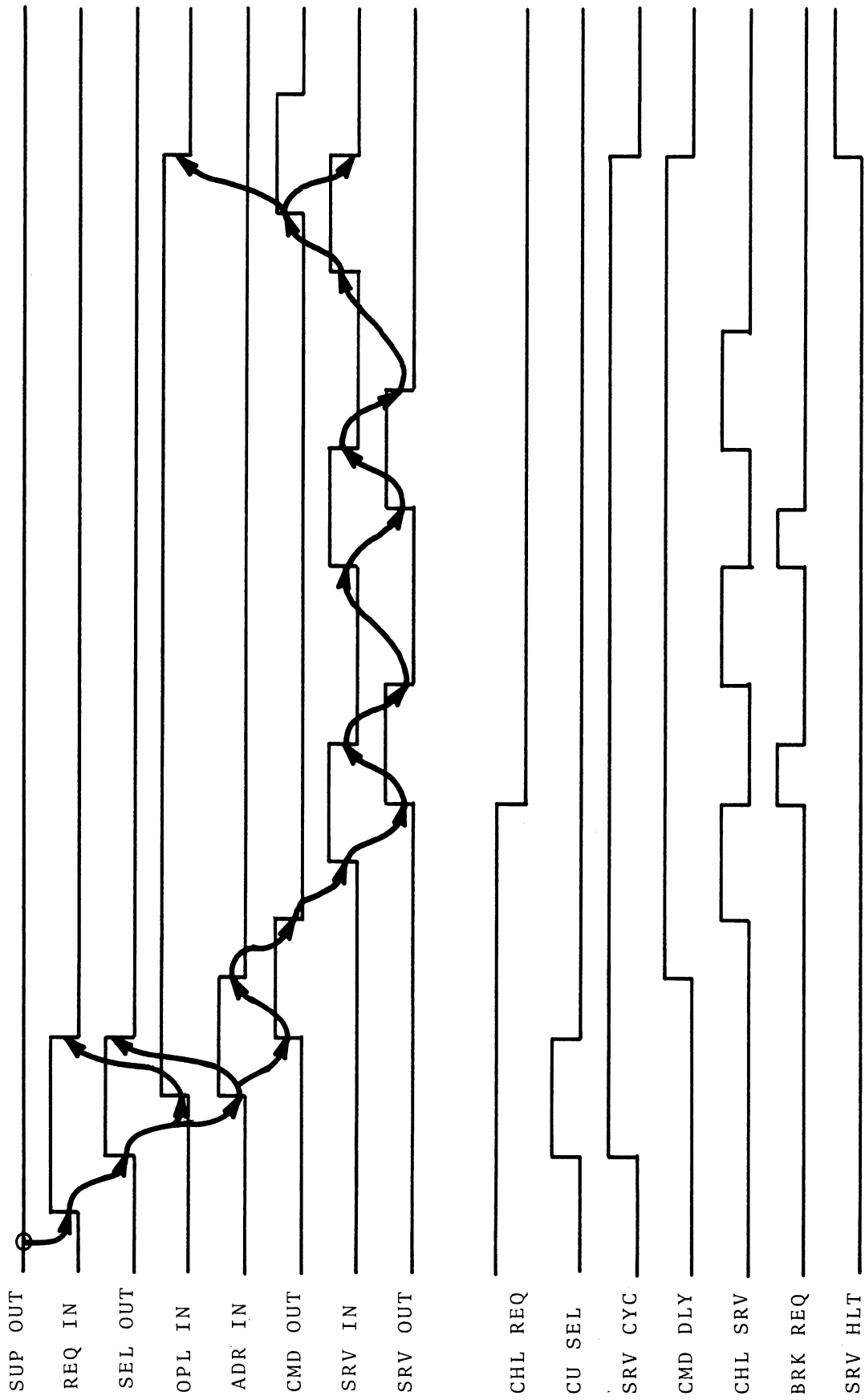
FIGURE 3. SERVICE CYCLE (BURST MODE)

        b.   SRV IN and places a data byte on BUS IN for transmission to the channel, or

        c.   raises SRV IN and waits for a SRV OUT channel acknowledgment that a data byte has been placed on BUS OUT for transmission to the control unit.

        If the device address does not have odd parity, the channel performs a malfunction reset. If a status byte does not have odd parity, an interface control check condition is generated. If, in the case of channel-inbound transmission, a data byte does not have odd parity, a channel data check condition is generated. Depending upon the particular machine model, these indications appear as a processor or memory check and as a bit set in the CSW stored as the result of the channel operation.

        The channel acknowledges the receipt of a data or status byte, as appropriate, with SRV OUT. This response is also used by the control unit to verify the presence of a data byte on BUS OUT where appropriate. The channel may alternatively respond to SRV IN with CMD OUT, indicating that the data region in its main storage is exhausted, and may respond to STA IN with CMD OUT, indicating that the status byte is to be stacked in the control unit for later presentation to the channel.

        In any case, the control unit responds to an outbound tag line at the end of the service cycle sequence by dropping all inbound tags and disconnecting from the interface. The channel is now free to continue polling for other control units on the interface or to issue new commands to the same or other control units. In particular, under some conditions, certain channel-generated commands may be directed to a busy control unit before device-end status has been serviced by the channel (see below).

3.3 Special Sequences

During the course of normal equipment operation and
in certain abnormal situations, special control-unit inter-
face sequences may be generated by the channel. These fall
into two classes: those intended to stop device activity by
request from the System/360 program, and those generated either by
manual intervention or by the machine itself for the purpose
of temporarily disconnecting the device from the system.

The first class of sequences includes the interface
disconnect sequence generated by the channel in response to a
Halt I/O (HIO) instruction executed by the System/360 program.
Such a sequence can occur at any time, either within an initial
selection or a service cycle sequence. The sequence is
signaled after the device address has been checked by the chan-
nel and when ADR OUT is up at the control unit while SEL OUT
is down. The sequence usually occurs before the command byte
is stored on initial selection, but may occur after CMD OUT
rises during a service cycle.

Figure 4 shows an interface disconnect sequence on
initial selection. Following such a sequence, the control
unit is expected to remove immediately all signals from the
interface and to present ending status following its device
operation. The ending status is to be transmitted only if
the associated System/360 subchannel was working at the time
of the sequence and may be cleared by a channel-generated TIO
command prior to program intervention.

The second class of sequences includes the selective
and system reset sequences generated by the channel in re-
sponse either to manual intervention or equipment malfunction.
The system reset sequence is indicated when both OPL OUT and
SUP OUT are down at any control unit. This sequence occurs
when power is first applied to the system, or when either the
SYSTEM RESET, LOAD, or PSW RESTART pushbuttons are depressed
on the System/360 operator's control panel. The selective

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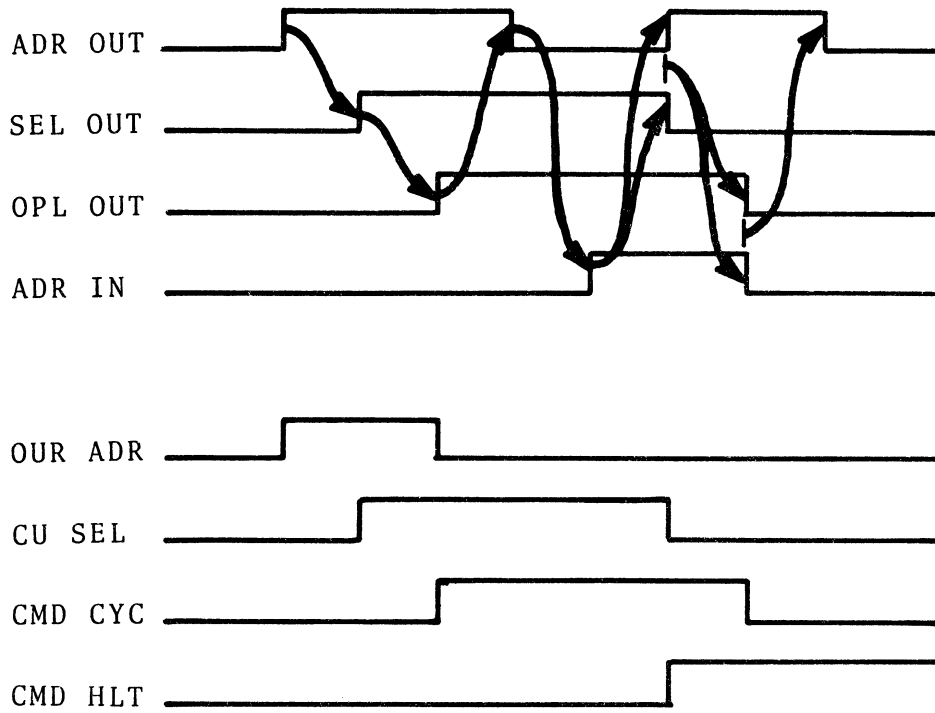
FIGURE 4.   INTERFACE DISCONNECT

reset sequence is indicated when OPL OUT is down while SUP OUT
is up at a control unit during an operation involving that
control unit. This sequence occurs when the channel has de-
tected a malfunction of the control unit or channel circuitry.
Such a malfunction may involve invalid BUS IN parity, improper
signal sequencing, or excessive sequence timings.

In the case of either the system or selective reset
sequences, the control unit is expected to disconnect from the
interface without presenting ending status for the operation.
Since the control unit may be reselected immediately following
a reset sequence, the control unit must appear busy to the
channel while any internal time-dependent reset operations
are completed.

3.4 Polling Operations

Since both the channel, its attached control units,
and their attached devices operate asynchronously with respect
to each other, conventions for device polling and acknowledg-
ment are required. The polling-acknowledgment conventions
appear at three levels:

a. during the initial selection of a control unit,

b. during the channel seizure procedure by a control
unit, and

c. during the selection and deletion procedures of a
device attached to a control unit.

Additional conflicts for both channel and subchannel access
by the System/360 program are resolved by the channel and in
some systems by the channel controller.

The channel selects an attached control unit with
the initial selection sequence. If the control unit is free
to accept a command (without respect to the status of its
attached devices), it responds with the sequence shown in
Figure 1. If not, then the control unit responds with the

control unit busy sequence shown in Figure 5. This sequence
begins in the same fashion as the initial selection sequence;
that is, the channel places a device address on BUS OUT and
raises ADR OUT. When SEL OUT rises at the control unit servic-
ing the device, and if the control unit is busy servicing some
other device, the control unit responds by placing a status
byte on BUS IN and raising STA IN. The channel responds with
SRV OUT unconditionally, following which the control unit
disconnects from the interface. Note that this sequence does
not require the control unit to store the device address
presented on BUS OUT or to present stored status for the de-
vice, even if it is available somewhere in the control unit.

The status byte presented to the channel during the
control unit busy sequence may take two forms. One form in-
cludes both the status modifier and busy bits, which by con-
vention inform the System/360 program that the control unit
is busy and will present a status byte containing the control
unit end bit at some future time. The other form includes
all three of these bits, which by convention inform the System/
360 program that the control unit is temporarily busy and that the
operation which was rejected by the control unit should be
immediately retried. The second form of status byte is used
when the control unit busy condition is expected to last some-
what less than a millisecond, the interrupt processing time of
typical System/360 programs, and the first form is used in all
other cases.

When the channel is not busy with some internal
operation and is not in the process of issuing an initial selec-
tion sequence directed to some attached control unit, the chan-
nel normally reverts to the polling mode. In this mode the
channel interprets REQ IN as a request to poll the interface
with SEL OUT, an operation that presumably will result in some
control unit raising OPL IN. In some models of the System/360
product line, the polling mode may be entered at interesting
times, for instance while the channel is retrieving the Channel
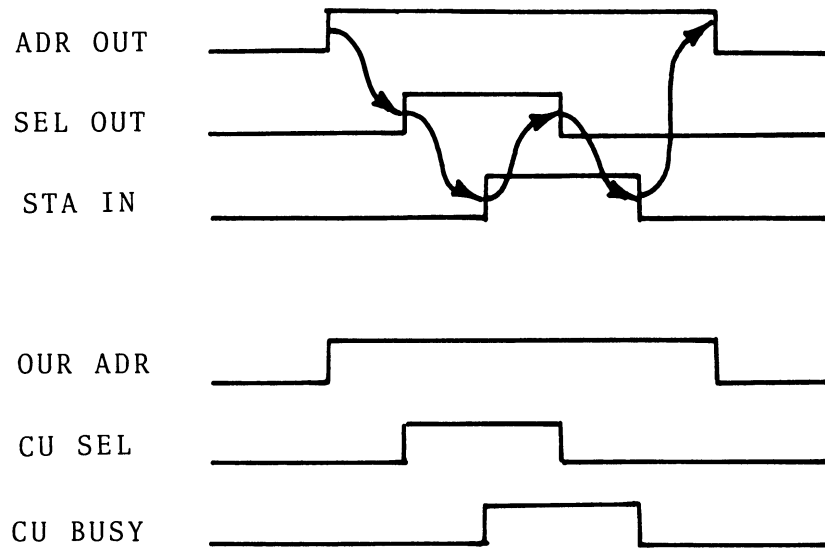
FIGURE 5. CONTROL UNIT BUSY

Address Word (CAW) or a channel command from main storage.
Since the System/360 CPU is interlocked between the time that
an I/O instruction is decoded and the time that the channel or
the addressed device responds, it is important that the control
unit sequence following REQ IN be as short as possible. In
extreme cases of control unit delay during a Start I/O (SIO)
operation (either addressed to the control unit or not), a
processor check may occur when the System/360 CPU microprogram
attempts to update its interval timer.

Data byte transmission operations for any particular
device take precedence over all other channel operations, and
are guaranteed to proceed without interference to the subchan-
nels connected to other devices serviced by the channel. Status
byte transmission operations, on the other hand, are considerab-
ly more involved and may take one of two alternate forms de-
pending upon whether the subchannel in question is busy or not.

An ending status presentation to a busy subchannel must
contain the channel end bit, but may contain others as well.
Such a status presentation will always be accepted by the chan-
nel with a SRV OUT response to a STA IN during the service
cycle. Once this status has been stored in local subchannel
storage, the channel requests a System/360 CPU interrupt which
causes a channel status word (CSW) containing the subchannel
status to be stored in main storage. An ending status presenta-
tion to a subchannel not in the busy state will be automatical-
ly stacked in the control unit with a CMD OUT response to a
STA IN tag during the service cycle. Before stacking the status
at the control unit, however, the channel stores the device ad-
dress of the requesting control unit in a special register
called the Interrupt Buffer (IB) (or Interrupt Queue). At this
time the channel requests a System/360 CPU interrupt, and, when
granted, causes a channel-generated pseudo-Test I/O command
to be issued to the device whose address is stored in the IB.
The control unit in question now furnishes this status as the
result of an initial selection sequence rather than the service

cycle sequence originally requested. Not all IBM control units can tolerate this interesting procedure; and, in fact, well-known machine hang-ups revealed in IBM documentation in connection with the 2702 Transmission Control are due to the failure of that device to process the pseudo-Test I/O.

3.5   Equipment Failure Diagnostics

Most control unit component malfunctions can be diagnosed by the channel; and, in many cases, the System/360 control program can recover from the malfunction condition, record the failure, and continue system operation. In the case of the programmable control unit equipment considered here, certain invalid programming sequences can also produce such malfunction indications to the channel. Six malfunction conditions are recognized by channel circuitry as probably originating in an attached control unit. These may or may not be detected separately or as distinct from a processor check, depending upon the machine model:

1.   Channel timeout. The System/360 CPU had not been released a pre-set interval (typically 150 microseconds) following issuance of an I/O instruction.

2.   Address-in check. The channel detected a parity error on the address received from the control unit during a service cycle.

3.   Status-in check. The channel detected a parity error on the status byte received from the control unit.

4.   Incorrect selection. The address received from the control unit during an initial selection sequence does not match that transmitted by the channel.

5.   No response. The control unit did not respond to re-selection on a chain-command operation.

6.   Incorrect tag sequence. The control unit disconnected from the channel before the channel dropped the SEL OUT tag line.

Any of these malfunctions cause the channel to assume an interface control check condition, which may be indicated as a bit set in the CSW stored as the result of the operation and further detailed in the log-out area peculiar to the model. Condition 6 can occur on the multiplex channel only as the result of an Initial Program Load (IPL) operation and will always be produced when such an operation is directed to a control unit such as the 2702 Transmission Control or the interface equipment described herein.

IV. PROGRAMMING CONSIDERATIONS
FOR IBM SYSTEM/360 INTERFACE

The System/360 interface is composed logically of two subinterfaces: the command interface and the service interface. The command interface stores the channel command and device address developed during the multiplex channel initial selection sequence and presents the appropriate status byte to the channel to terminate the sequence. At the conclusion of the sequence, appropriate bits are set in a control register to indicate the particular type of sequence to the PDP-8 interrupt processor. The service interface supervises data break operations between the PDP-8 and the multiplexor channel. This interface is started by the PDP-8 program by loading a three-bit command code in the control register, following which three-cycle data break operations occur for data transmission between a block of PDP-8 memory and the channel. Both data and ending-status bytes are transmitted in this fashion. At the conclusion of the operation, either at channel-stop or word-count-equal-zero times, bits are set in the control register to indicate the termination condition to the PDP-8 interrupt processor.

Five registers in the interface are available to the PDP-8 program. Two of these, AR1 and BR1, are used in connection with the command interface, while another two, AR2 and BR2, are used in connection with the service interface.

The fifth register, CTL, is common to both interfaces, and serves as the controlling element for the various operations. The AR1, BR1, and AR2 registers can be read, cleared, and loaded (one's-transfer) from the AC of the PDP-8. The BR2 register is connected only to the data break facility. The CTL register can be read, inverted, and tested bit-by-bit with appropriate microinstructions (see below). Some of these registers need not be read or loaded during the common interface operations; the general read/load facility is included primarily for diagnostic utilities. Figure 6 illustrates the coding of the various register bit assignments and establishes the IOT microinstruction codes for their access.

The operation of the control register invert-under-mask (CTL INV) and test-under-mask (CTL TST) microinstruction is as follows: Both of these instructions address the twelve control register bits in one-to-one correspondence with the bits of the AC. The operation of the CTL INV microinstruction results in a bit-wise inversion of each bit in the control register for which the corresponding bit in the AC is a one. The operation of the CTL TST microinstruction results in a single-instruction program skip if each control register bit which is in correspondence with a one bit in the AC is a one. If any control register bit in correspondence with a one bit in the AC is a zero, no program skip is generated. An unconditional skip is generated if the AC contains all zeros.

The RD, CLR, and WR modifiers may be applied to the registers designated AR1, BR1, and AR2. The sequence of the IOP pulses is such that the micro-operations are performed in the order listed. The RD, TST, and INV modifiers may be applied to the register designated CTL. The micro-operations are performed in that order. Appendix F illustrates segments of code that are applicable in common programming situations.
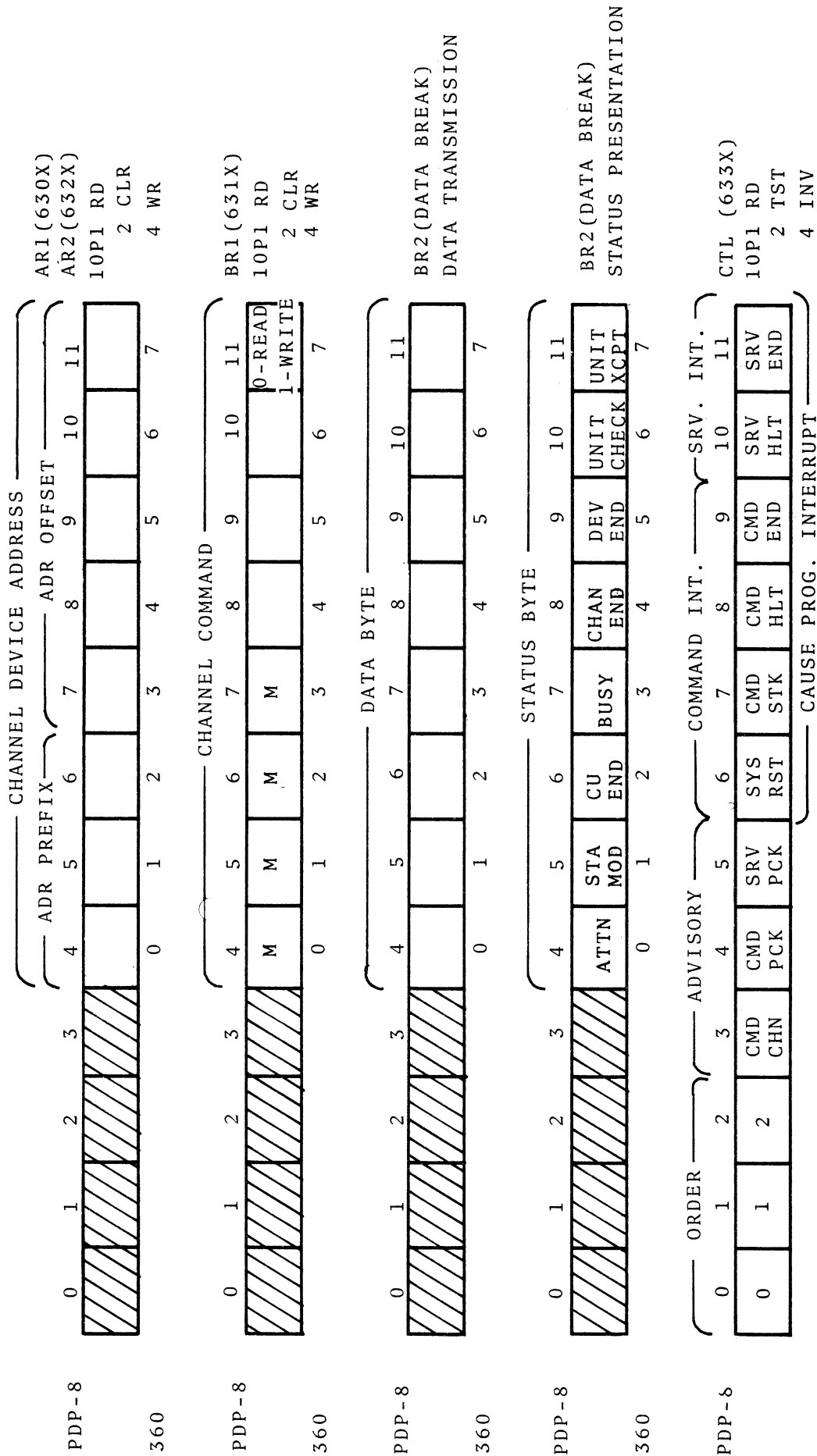
FIGURE 6. REGISTER BIT ASSIGNMENTS

4.1 Command Interface Operations (Figure 7)

Three of the four System/360 I/O instructions will
result in a channel sequence in the command interface, and
two of these will normally end by interrupting the PDP-8 pro-
gram. An SIO instruction executed by the System/360 will result
in one or more channel commands being fetched from System/360
core storage and transmitted to a control unit. If the device
address specified in the SIO instruction lies within the block
recognized by the command interface and if the interface is not
busy (i.e., holding a previously issued command), then the inter-
face will seize the channel and store the device address in AR1
and the command byte in BR1. If the channel sequence is gener-
ated as a result of a valid channel command, the command byte
stored in BR1 must be nonzero, and will be an odd number if
channel-outbound service is indicated and an even number if
channel-inbound service is indicated.

Note that in order for the selection sequence to be
initiated, the parity of the device address must be odd. If
this parity is odd and yet the parity of the command byte is
not odd, then the CMD PCK bit of the control register is set.
This situation, interpreted as a BUS OUT parity check, does
not affect the progress of the selection sequence or the status
byte subsequently transmitted to the channel.

At the conclusion of the initial selection operation,
the CMD END bit of the control register is set if the channel
accepted the interface-generated all-zero status byte and
the CMD STK bit if the channel rejected the byte. If the
channel sequence is generated as the result of a valid channel
command, an occurrence of the later situation must be inter-
preted as a System/360 machine check.* When either the CMD END
or CMD STK bits are set, the PDP-8 is interrupted.

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* Note that in current System/360 channel equipment, stack on
   initial selection (CMD STK) never occurs on an all-zero
   status byte. In the case of a nonzero status byte, stack on
   initial selection will be generated only in certain cases
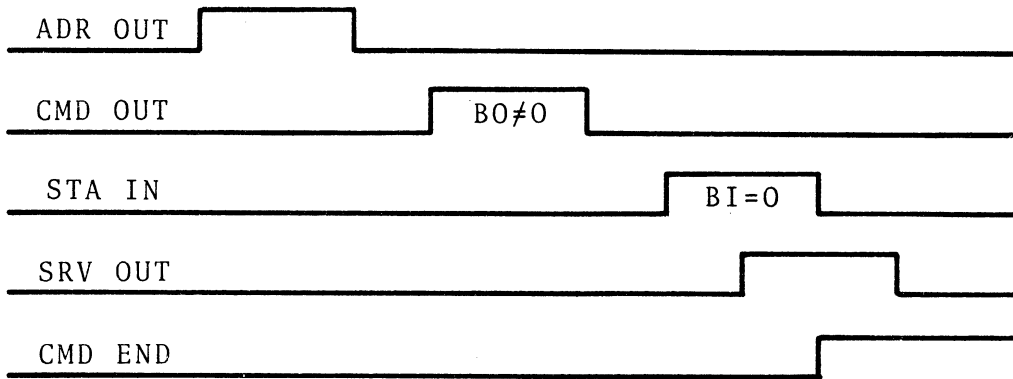
INITIAL SELECTION—STATUS ACCEPTED
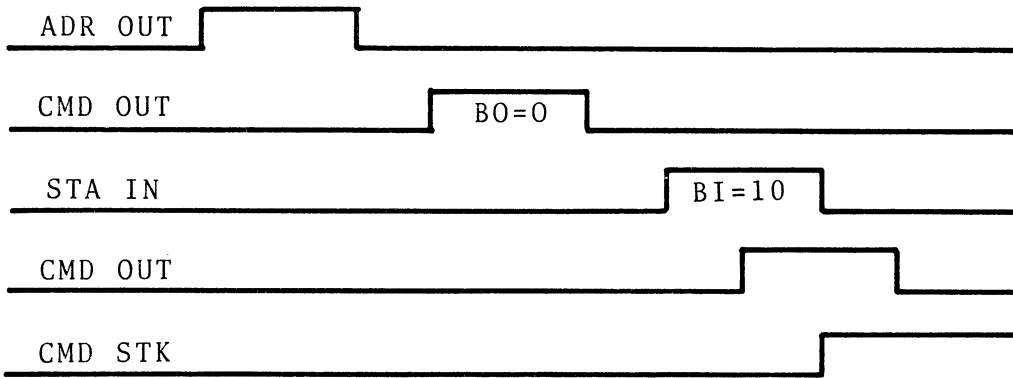
INITIAL SELECTION—TIO STATUS STACKED
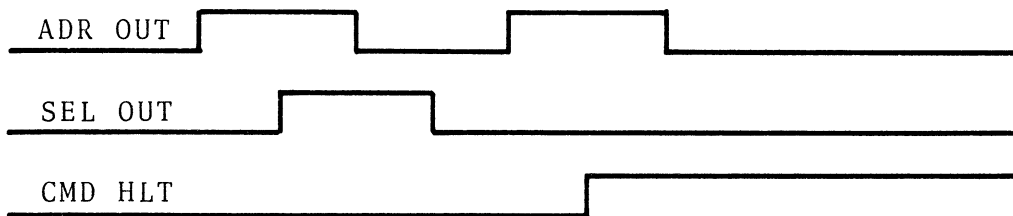
INITIAL SELECTION—HIO

FIGURE 7.

A Halt I/O (HIO) instruction executed by the System/360 causes a special channel sequence to be transmitted to a control unit. If the device address specified in the HIO instruction lies within the block recognized by the command interface and if the interface is not busy, then the interface will seize the channel and store the device address in AR1. BR1 will be forced to an all-zero byte. This sequence ends by setting the CMD HLT bit of the control register. A selective reset sequence generated by the channel during the progress of any command interface operation will also set this bit.** When the CMD HLT bit is set, the PDP-8 is interrupted.

A Test I/O (TIO) instruction executed by the System/360 causes a special channel sequence which is identical to the SIO sequence except that the command byte contains only zero bits. If the device address specified in the TIO instruction lies within the block recognized by the interface and if the interface is not busy, then the sequence ends by the transmission to the channel of a status byte containing only the status-modifier bit. If the channel accepts this byte, the interface is released and the PDP-8 is not disturbed. If the channel rejects the status byte, then the CMD STK bit is set in the control register and the PDP-8 program is interrupted. It is the responsibility

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involving command chaining. Since the command interface generates a nonzero status byte only in response to a Test I/O instruction, and since this "instruction" may not occur as an element of a channel-command sequence, it is not at all clear from extant documentation whether the CMD STK bit can ever be set in any likely programming situation.

** A selective reset sequence is generated by channel equipment, at least in some models, in response to a status presentation of bad parity and possibly in response to an invalid tag-line sequence. A presentation of a device address of bad parity in conjunction with ADR IN will usually result in a channel-generated system reset sequence. A presentation of a data byte of bad parity is not always detected by the channel itself, but may be detected by the CPU or memory bus register circuitry and cannot be differentiated from parity errors due to other causes.

of the PDP-8 program to retransmit a status byte containing
the status modifier bit via the service interface when allowed
by the channel (however, see preceding footnote). Note that
this behavior in connection with the TIO instruction is con-
sistent with that of the IBM 2702 Transmission Control and
implies, in particular, that the command interface cannot pro-
vide status in response to a program-generated TIO instruction.
Note further that pseudo-TIO instructions can be generated by
the channel without intervention by the program, and in these
cases the command and service interfaces must cooperate in the
successful transmission of a status byte to the channel. Such
situations arise in connection with ending-status transmissions
to subchannels not in the busy state (see below).

If a system reset sequence is generated by the chan-
nel, either as the result of power-up, initial program load,
or manual operator intervention, the CMD RST bit of the control
register is turned on. This operation clears all other bits
of the control register and results in a PDP-8 program inter-
rupt. All System/360 registers and subchannels are reset and
placed in the available state. Pending data and status trans-
missions on the part of the PDP-8 should be suspended.

If any System/360 channel operation is directed to
the command interface when either the CMD STK,CMD RST,CMD HLT,
or CMD END control register bits are set, the command inter-
face will immediately reject the operation with the control
unit busy sequence, which involves the transmission to the
channel of a status byte containing the status modifier, busy,
and control unit end bits. This sequence is by convention
interpreted by both the channel and the System/360 program
as an indication to immediately retry the operation. For this
reason, the resident PDP-8 program should give high priority
to command interface interrupts, since the System/360 program
may be hung up during the response interval. The PDP-8 in-
terrupt processor clears such interrupts by inverting the

appropriate bit of the control register to a zero. Previous
to this operation, meaningful contents of both the AR1 and
BR1 register must of course be preserved in core storage by
the interrupt processor. It is possible in some System/360
programming systems that tight TIO or HIO loops may be exe-
cuted under certain conditions. In the case of the HIO instruc-
tion, the resultant load on the command interface will most
certainly lock up the PDP-8 interrupt processor, which then
must clear the System/360 condition, presumably by the trans-
mission of ending status to the channel. In any case, the
PDP-8 program must be aware of situations inherent in the
particular parent System/360 supervisory programming system
in which TIO or HIO loops are involved or in which the multi-
plex channel is masked against interrupts, and must give high
priority to channel service under those conditions.*

4.2 <u>Service Interface Operations</u> (Figure 8)

In all service-interface operations, a block of data
is transferred either channel-inbound or channel-outbound.
The three-cycle data break facility of the PDP-8 is used for
this block transfer operation, which once initialized by the
PDP-8 program, continues until the PDP-8 residual word
count decrements to zero, until the channel detects
that a System/360 core memory storage area is exhausted,
or until the System/360 program issues an HIO instruction. All
transmission operations make use of only the low-order eight

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* A typical instance of a tight TIO loop occurs after present-
  ation of a unit check to certain present System/360 pro-
  gramming systems. Programming constraints imposed by other
  control units, in particular the 2841, require that a TIO be
  directed to the control unit immediately following a unit
  check. In such a case, the selector channel must be disabled
  before issuance of the TIO. In such cases, the same behavior
  may exist on the multiplexor channel, a behavior which is
  strongly disadvised, since not only the command interface
  but other IBM control units as well will hang up the system
  for some time.
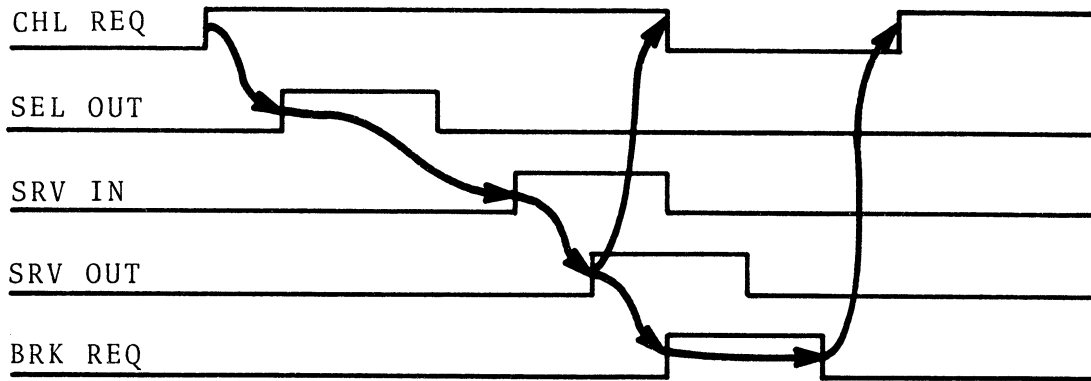
SERVICE CYCLE (BYTE-INTERLEAVED MODE)
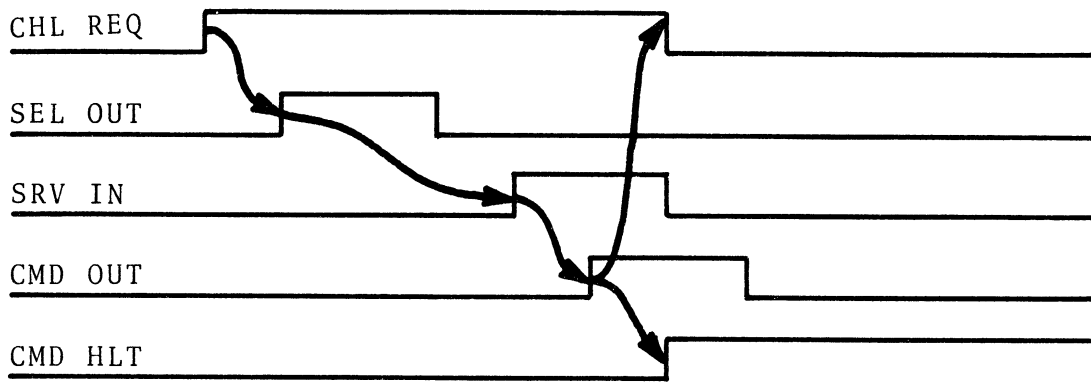
SERVICE CYCLE-STOP

Figure 8a.
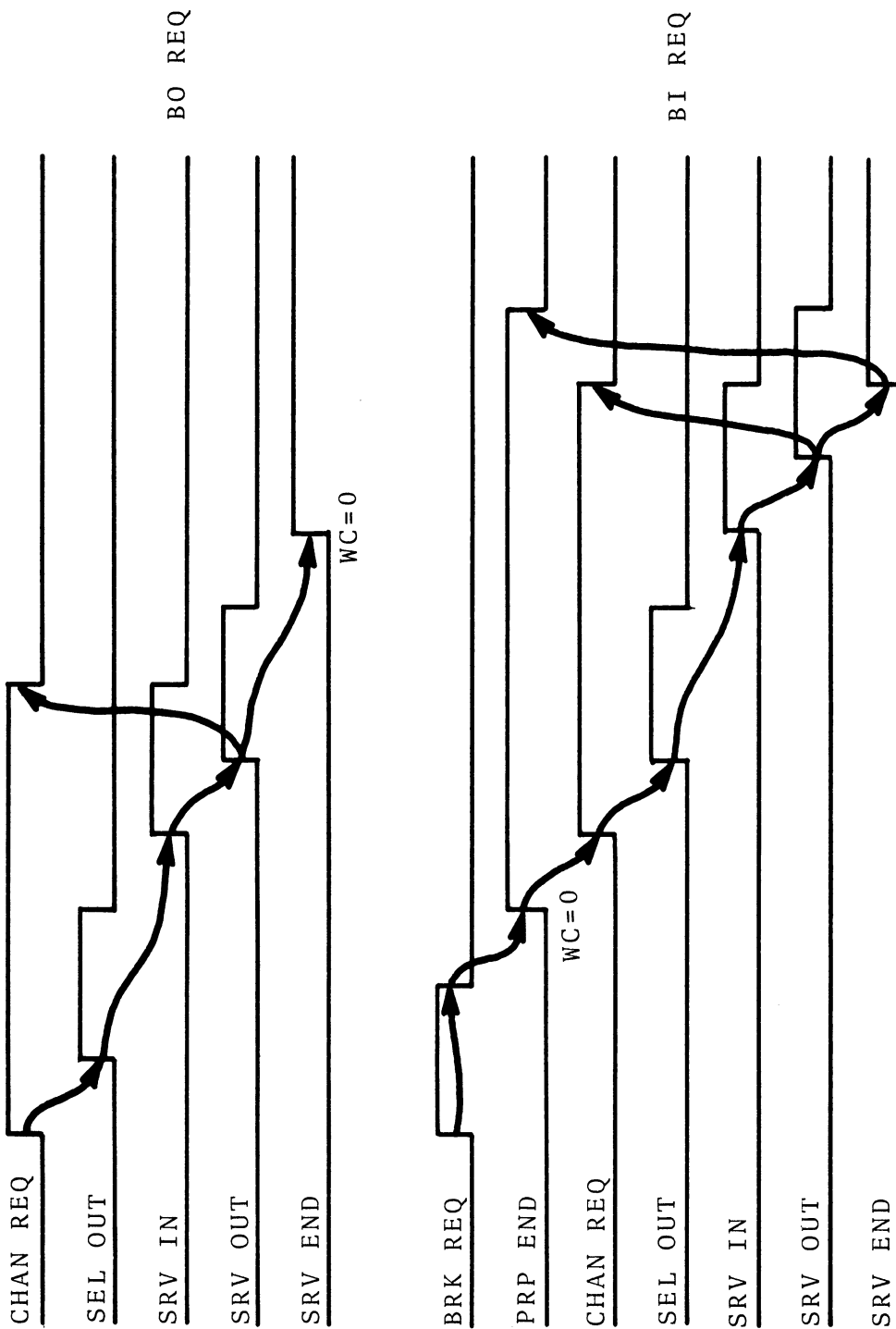
SERVICE CYCLE—END

FIGURE 8b.

bits of a PDP-8 core memory location. The four high-order
bits are ignored in channel-inbound operations, and are re-
placed by zeros in channel-outbound operations. Either data
bytes or status bytes may be transferred using the appropriate
interface order codes (see below). In the case of status byte
transmission, the service interface will automatically re-
present status to the channel following a stack-status channel
sequence.

All data and most status operations involving the
service interface take place only when the associated System/
360 subchannel is busy, that is when a valid channel command
has been stored by the command interface. If the low-order
bit of the channel command is a zero, then channel-inbound
service is requested and the PDP-8 program must select the
interface-outbound data operation. If the low-order bit of
the channel command is a one, then channel-outbound service
is requested and the PDP-8 program must select the interface-
inbound data operation. Violation of these constraints will
usually result in either a channel check, processor check,
or storage check, depending upon the particular System/360
model.

Status presentation to the channel when the sub-
channel is busy will not usually be stacked by the channel;
and, if a status presentation happens to be stacked, it can
eventually be cleared by re-presentation to the channel. If
the subchannel is available to the System/360 program, then
any status presentation will be automatically stacked and
must be cleared by a channel-generated pseudo-TIO command.
Such considerations dictate a careful organization of the
PDP-8 program to avoid System/360 hangups due to conflicts
at the command and service interfaces.

All service interface operations involve a pro-
grammed procedure which

a. presets the word count and current address loca-
tions accessed by the three-cycle data break facility,

b. loads AR2 with the specified device address,
and finally

c. loads a three-bit order code into the control
register.

The service interface then proceeds with alternate channel
sequences and three-cycle data break operations until either
the PDP-8 word count is decremented to zero, or until a stop
sequence is generated by the channel. The appropriate bits
are then set in the control register and the PDP-8 program
is interrupted. The interrupt is cleared by inverting the
appropriate control register bits to zeros.

In the case of data operations, operation can be
selected in either the byte-interleaved or burst mode. The
byte-interleaved mode is appropriate for either low-speed
operations with all models or both low- and high-speed opera-
tions with the higher-numbered models. Depending upon the
width of the data paths to core memory and the degree of CPU
involvement in the multiplexor channel operations, the burst
mode may be appropriate for high-speed operations with the
lower-numbered models.

A channel-outbound byte-interleaved data operation
is started by loading an octal 2 into the high-order three
bits of the control register. An octal 3 starts the same
operation in burst mode. These orders initiate a data opera-
tion from the channel to the PDP-8 core memory. When the
PDP-8 word count decrements to zero, the SRV END bit is set
in the control register. When a stop sequence is transmitted
by the channel in response to a service request by the inter-
face,the SRV HLT bit is set in the control register. No
data byte is transmitted to the PDP-8 core memory on a SRV
HLT cycle.

This operation is suppressible. That is, if the channel is undergoing some critical sequence which should not be interrupted for lower priority operations, the service interface will suspend data transmission. Such is the case when another control unit on the channel is operating in burst mode or when certain status operations are pending at the channel. If an operation is not outstanding in the System/360 subchannel addressed by AR2, then, depending upon the model, the channel will either respond unconditionally with a stop sequence or an interface disconnect sequence, either of which sets the SRV HLT bit of the control register, or hang up the channel. If a data byte presented by the channel does not have odd parity, then the SRV PCK bit is set in the control register. This condition does not affect the further progress of the operation and in particular does not cause a PDP-8 program interrupt.

A channel-inbound byte-interleaved data operation is started by loading an octal 4 into the high-order three bits of the control register. An octal 5 starts the same operation in burst mode. This order initiates a data operation from the PDP-8 core memory to the channel. When the PDP-8 word count decrements to zero, the SRV END bit is set in the control register. The last byte fetched from PDP-8 memory on the SRV END cycle is transmitted to the channel. When a stop sequence is transmitted by the channel in response to a service request by the interface, the SRV HLT bit is set in the control register. The last byte obtained from PDP-8 memory on a SRV HLT cycle is then lost whether or not the SRV END bit is set during the same cycle.

The comments above under channel-outbound data transmission concerning data suppression and operation with an available subchannel apply also to channel-inbound data transmission. Odd parity is automatically generated on all channel-inbound operations whatever their nature, and the SRV PCK control-register bit is never affected by such operations.

When either the SRV END or the SRV HLT control reg-
ister bits become set as a result of a service interface
operation, the PDP-8 program is interrupted. The interrupt
processor can determine how many data bytes have been success-
fully transmitted by inspecting the residual word count
stored by the three-cycle data break facility and applying the
modifying factors shown in Table 1. If the SRV HLT bit is
not on at the conclusion of an operation, the opportunity
exists to transmit additional data blocks. If both the
SRV HLT and SRV END bits are set in the control register
following a channel-outbound data operation, an interface
failure is evident.

At the conclusion of the transmission of all data
blocks, and in any case following any operation terminated
by the SRV HLT bit, a status presentation is expected by the
channel. Such a presentation must include the channel end
bit and may include others as well. Following the presenta-
tion of channel end, the subchannel involved reverts to the
interruption-pending state and may allow certain I/O instruc-
tions addressing the subchannel to proceed directly to the
command interface. The subchannel reverts to the available
state upon receipt of an interrupt response from the System/
360 CPU, following which any I/O instruction may be directed
to the command interface. The channel end and device end
bits may be combined in a single status byte.

A standard status operation is one in which a status
byte containing the channel-end bit is to be transmitted to a
working subchannel. Such an operation is started by loading
an octal 7 into the high-order three bits of the control
register. This order initiates a status operation involving
status byte transmission from the PDP-8 core memory to the
channel. Usually only one byte will be transmitted to the
channel on any one operation; but, regardless of the number
of bytes actually transferred, the operation can legitimately
terminate only when the PDP-8 word count decrements to zero,

TABLE I

Order	SRV HLT	SRV END	Sequence	*Bytes Transmitted
Data Outbound				
CTL 2	0	1	PDP-8 stop	N-W
CTL 3	1	0	channel stop	N-W
	1	1	not possible (see text)	—
Data Inbound				
CTL 4	0	1	PDP-8 stop	N-W
CTL 5	1	0	channel stop	N-W-1
	1	1	channel stop on last byte	N-W-1
Status Inbound				
CTL 6	0	1	PDP-8 stop	N-W
CTL 7	1	0	not possible (see text)	N-W-1
	1	1	not possible (see text)	N-W-1

* N = initial word count
  W = residual word count

a condition that sets the SRV END bit in the control register
and interrupts the PDP-8 program. If an interface disconnect
or selective reset sequence is transmitted by the channel in
response to a status presentation, then the interface will
immediately disconnect from the channel and cause the
SRV HLT bit to be set in the control register.

The standard status operation is not suppressible
by the channel. That is, status presentations cannot be
locked out of the system if the channel is disabled but
has an interrupt pending for another device. Under
these conditions, a TIO instruction issued by the System/360
program can clear pending status at the service interface.
Such a procedure is called for following presentation of unit
check in a status byte to certain System/360 programming
systems (see preceding footnote). Such systems regularly
follow presentation of unit check by a Sense channel command
while the channel is disabled, and rely on clearing device
status using a TIO loop. Note that in such cases a busy
indication is returned to the System/360 program as long
as the subchannel is working; and, in particular, the TIO
is not propagated to the device itself. Thus, if the
subchannel is working, a standard status operation will
always terminate with the channel accepting the presentation
by the service interface, and in particular without the
generation of pseudo-TIO commands on the part of the channel.

If a standard status presentation is once stacked
by the channel for any purpose, then the interface itself
automatically "demotes" the priority to that of a special status
presentation. A special status operation is one in which a
status byte is to be transmitted to a subchannel not in the
working state. That is, a subchannel in either the available
or interruption-pending states. Such an operation is started
by loading an octal 6 into the high-order three bits of the
control register. This order initiates a status byte trans-
mission in the same manner as the standard operation, with

the exception that the presentation is suppressible by the channel. Such behavior is necessary to avoid the lockout of a channel-end status presentation of a lower-priority control unit on the channel interface cable by an unsolicited status presentation by the service interface. As in the standard operation, the special operation ends by setting the SRV END bit in the control register.

To summarize the application of the two kinds of status operations, the standard operation is used to transmit a status byte, which must contain the channel-end bit, to a working subchannel; and the special operation is used to transmit a status byte to a non-working subchannel. A failure to make this distinction will result in a machine hangup in the lower-numbered models of the System/360 product line and in an interface control check (channel timeout) in the higher-numbered models. Such situations may result in a diagnostic Channel Status Word (CSW) to be stored by the System/360.

If SUP OUT is up when SRV OUT is raised by the channel in response to an ending status presentation, the CMD CHN bit of the control register is set. Such an action is interpreted as an indication that the channel is command-chaining the previous operation and is about to reselect the interface for issuance of a new channel command. The indication of the CMD CHN bit is only advisory to the PDP-8 program and does not affect the progress of any channel or interface sequence. Depending upon the circumstances involved, the PDP-8 program may process this indication as a request to save such status presentations as the attention bit until the end of the System/360 channel program, or to assign high priority to command interface operations so that the immediately following reselection procedure will not delay the channel.

4.3   System/360 Control Program Operations

Interface programming considerations for the System/ 360 resident control programs are similar to those for the 2702 Transmission Control. However, due to the somewhat richer architecture of the interface, the behavior of the two machines will be slightly different. The main differences are:

1. channel-end and device-end status presentation do not necessarily have to occur in the same byte,

2. burst-mode operation can be sustained,

3. no immediate channel command operations are possible,

4. unsolicited status presentations are possible.

Considerations 1 and 2 imply that it is possible to use the interface on a shared subchannel, effecting a cost reduction in channel equipment on some models. However, since it is not possible to determine at initial selection time whether a particular device attached to the PDP-8 and logically connected to a particular System/360 subchannel can or cannot accept a channel command (consideration 3), use of this capability would be rather awkward. Consideration 2 implies that system performance at moderate data rates can be materially improved in the lower-numbered models by programming the PDP-8 to operate in short multi-byte bursts. The System/360 programming problems in connection with burst-mode operations are similar to those arising in connection with tape control unit operations on the multiplexor channel. Consideration 3 is another implication of the general interface characteristic that all commands are accepted if the interface is not busy. Consideration 4 is an implication of the capability of the interface to clear asynchronous unsolicited status presentations as the result of a pseudo-Test I/O instruction.

Following is a short summary of the operation of
System/360 I/O instructions when directed to a device ad-
dress recognized by the interface. Only those features of
operation dependent upon the peculiar characteristics of
the interface are emphasized.

Start I/O

Issued to a nonworking channel and subchannel,
this instruction will always result in a command interface
operation involving the transmission of a channel command to
the interface. If both the command and service interface
are idle before transmission of the channel command, then
condition code 0 is set at the conclusion of the Start I/O
operation. I/O activity is begun and the subchannel is
placed in the working state. If the command interface is
busy, then condition code 1 (CSW stored) is set at the con-
clusion of the operation. The device status field of the CSW
contains the busy, control unit end, and status modifier
bits. No I/O activity is started and the command interface
is undisturbed following this operation. Normally the in-
dicated busy condition may be expected to last in the order
of a few hundred microseconds, representing the interrupt
processing time of typical PDP-8 programs. If the command
interface is idle and the service interface is holding
pending status for the device addressed by the Start I/O
instruction, then condition code 1 is set at the conclusion
of the operation. The device status field of the CSW con-
tains the status presented by the service interface and in
addition the busy bit. No I/O activity is started and both
the command and service interfaces are idle following the
operation.

Halt I/O.

Issued to a nonworking channel, this instruction
will always result in a command interface operation without
regard to the state of the subchannel. In addition, the

subchannel will be set up to signal the service interface to stop data transmission the next time a service cycle is requested. If the command interface is idle prior to the issuance of a Halt I/O instruction, then condition code 1 is set at the conclusion of the Halt I/O operation and the status field of the CSW is replaced with zeros. I/O activity is stopped by the addressed device, which will then provide ending status under control of the resident PDP-8 program. If the command interface is busy, then condition code 1 is also set following the operation, but the status field of the CSW contains the busy, control unit end, and status modifier bits. The Halt I/O indication has not been stored by the command interface, although the subchannel is set up to signal this condition when the service interface next requests a service cycle.

Test I/O

Issued to a nonworking channel and subchannel, this instruction will always result in a command interface operation but will not affect the PDP-8 program unless status presented is stacked by the channel. (And whether this can ever happen is highly dubious—see comments elsewhere in this document.) Condition Code 1 will always be stored at the conclusion of the Test I/O operation. If the command interface is busy prior to the issuance of this instruction, then the status field of the CSW will contain the busy, control unit end, and status modifier bits. If the command interface is idle and status for the addressed device is available at the service interface, then that status replaces the status field of the CSW. If neither of these conditions hold, then the single status modifier bit is placed in the status field of the CSW.

Programming Notes

Contrary to published doctrine, it is evidently possible to cause I/O interrupts from devices whose subchannels are working, but without including the channel end bit and without affecting the status of the subchannel. It is not at all clear whether this is possible on all models or whether unknown machine incompatibilities can occur. Use of this feature (for instance as an attention interrupt) in real-time control environments is obvious.

In some programming systems, an automatic Sense channel command is issued (with channels disabled) when a unit check bit is set in a status byte. These systems rely on a Test I/O loop to clear ending status from the Sense command. If the Test I/O loop is looking for device end, then the cooperating PDP-8 program must present channel end and device end together on the status byte which ends the Sense command. Alternatively, the PDP-8 program must arrange that a channel end status presentation for a particular device address be followed only by status pertaining to the same device. Otherwise conflicts between the channel and the interface can occur in which the channel is asking for status (via a programmed or pseudo-Test I/O) for a device that the service interface is just not prepared to surrender.

V. ARCHITECTURE OF SYSTEM/360 INTERFACE*

The System/360 interface contains the registers and control circuitry to provide a bidirectional asynchronous transmission of both command, status, and data bytes between the System/360 multiplexor channel and the PDP-8. The interface consists of four data registers, their transfer gates, a control register, and various sequencing circuitry. The organization of these components is shown in Figure 9.

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* Logic symbology in this section corresponds to IBM standard usage. See Preface.
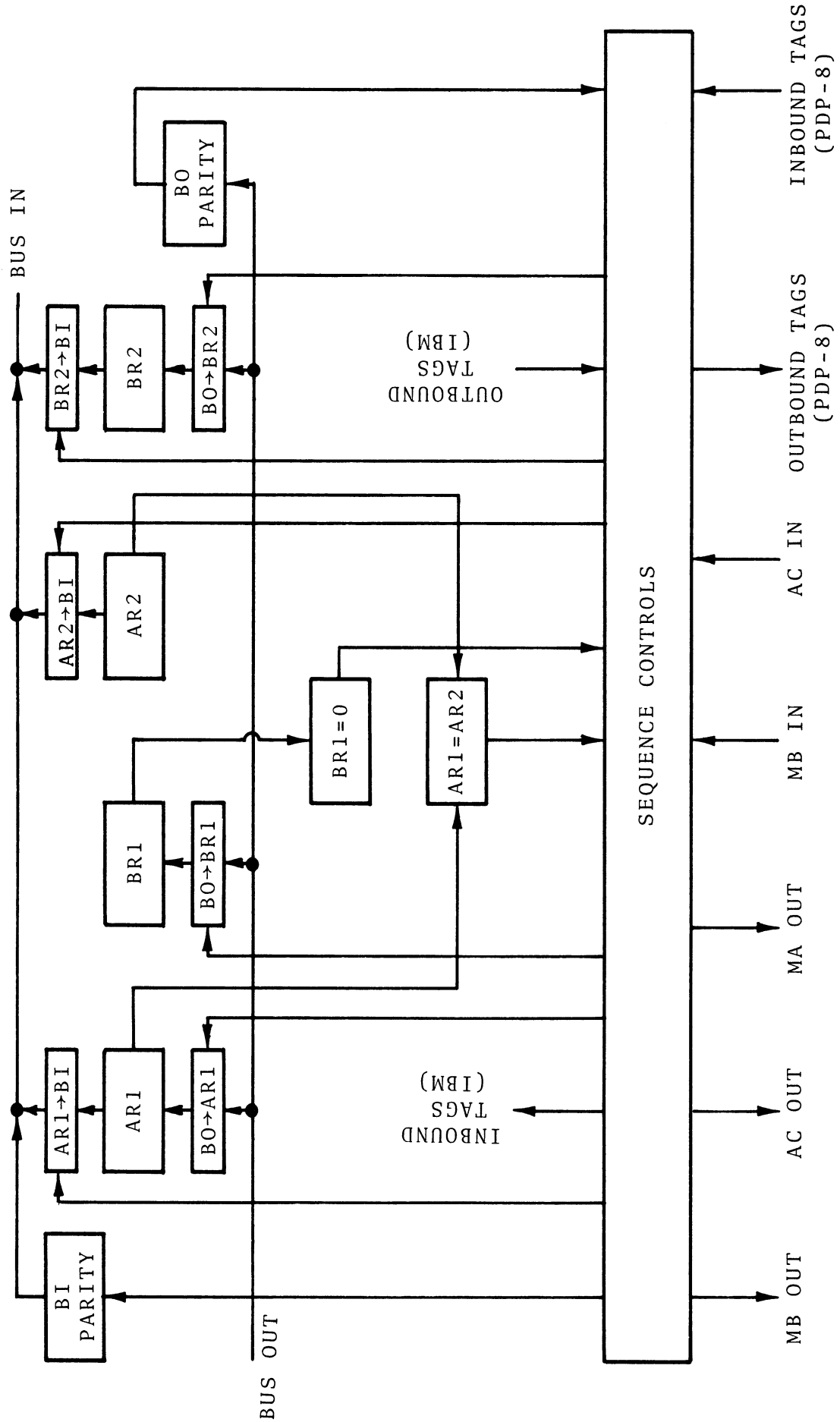
FIGURE 9. PRINCIPAL INTERFACE COMPONENTS

Referring to Figure 9, the four data registers are designated Address Register 1 (AR1), Buffer Register 1 (BR1), Address Register 2 (AR2), and Buffer Register 2 (BR2). All four registers are provided with jam-transfer direct-coupled diode-capacitor-diode (DCD) gates from the test switches, and, in addition, all except BR2 are provided with ones-transfer DCD gates from the PDP-8 AC. AR1 is used to hold the device address presented by the channel during the initial selection sequence and is provided with jam-transfer direct-coupled (DC) gates from BUS OUT. BR1 is used to hold the command byte presented by the channel during the initial selection sequence and is provided with ones-transfer DC gates from BUS OUT. AR2 is used to hold the device address presented to the channel during a service cycle. No inbound transfer gating is provided except for the DCD gates mentioned above. BR2 is used to hold a status or data byte during a service cycle and is provided with ones-transfer DCD gates from the PDP-8 MB and with ones-transfer DC gates from BUS OUT. BUS IN is provided with ones-transfer DC gates from AR1, AR2, and BR2 as well as constant generators 10, 40, and 70 (hex), which are used to synthesize certain status bytes. The PDP-8 AC is provided with a special set of ones-transfer DC gates called the EAC bus, which is in turn provided with ones-transfer DC gates from AR1, BR1, and AR2. The EAC bus is used both to isolate the PDP-8 AC bus from the loading of the transfer gates and to provide a uniform interface for additional equipment, other than the interface, which may be connected to the PDP-8. The PDP-8 MB is provided with ones-transfer gates from BR2. These gates are used in connection with a special data multiplexor described elsewhere.

A nine-bit parity detector connected to BUS OUT indicates that odd parity is present on these lines and is used in conjunction with AR1, BR1, and BR2 when these registers are loaded from BUS OUT. A parity error during the

BR1 or BR2 loading operation will set the CMD PCK or SRV PCK bits of the control register respectively. An eight-bit parity generator connected to the BUS IN transfer gates provides odd parity for the BUS IN (P) line and is used in conjunction with all BUS IN operations.

An eight-bit zero detector connected to BR1 is used during the initial selection sequence to detect the occurrence of a Test I/O channel command and to condition the following BUS IN status accordingly. An eight-bit compare circuit is connected to AR1 and AR2 to detect when these two registers contain identical bits and is used during the pseudo-TIO status sequence.

A three-bit decoder connected to BUS OUT is used during the initial selection sequence to determine whether the device address present on BUS OUT falls within the block serviced by the interface. Eight blocks of addresses, each consisting of a contiguous block of 32 addresses, may be selected by a jumper card.

The twelve-bit Control Register (CTL) is composed of a three-bit Order Register (OR) and a nine-bit Status Register (SR). The OR is used to hold the order code during a service cycle and is automatically reset following the conclusion of a block transfer operation. The SR is used to hold the various bits that indicate termination conditions of the interface sequences. However, the SR has no direct connection with any status byte that may be presented to the channel.

The logical details of these registers and their transfer gates are shown in Figure 10. Figure 11 shows the logical details of the PDP-8 data paths, and Figure 12 shows those of the BUS IN data paths. Circuit names, which appear only in this simplified description, are indicated on these diagrams. In some cases the actual circuit names and logical details differ from those recorded here. The logical details of the circuitry for all of these components are straightforward and are recorded in Appendix E. The logical organization of the control and sequencing circuitry, however, is
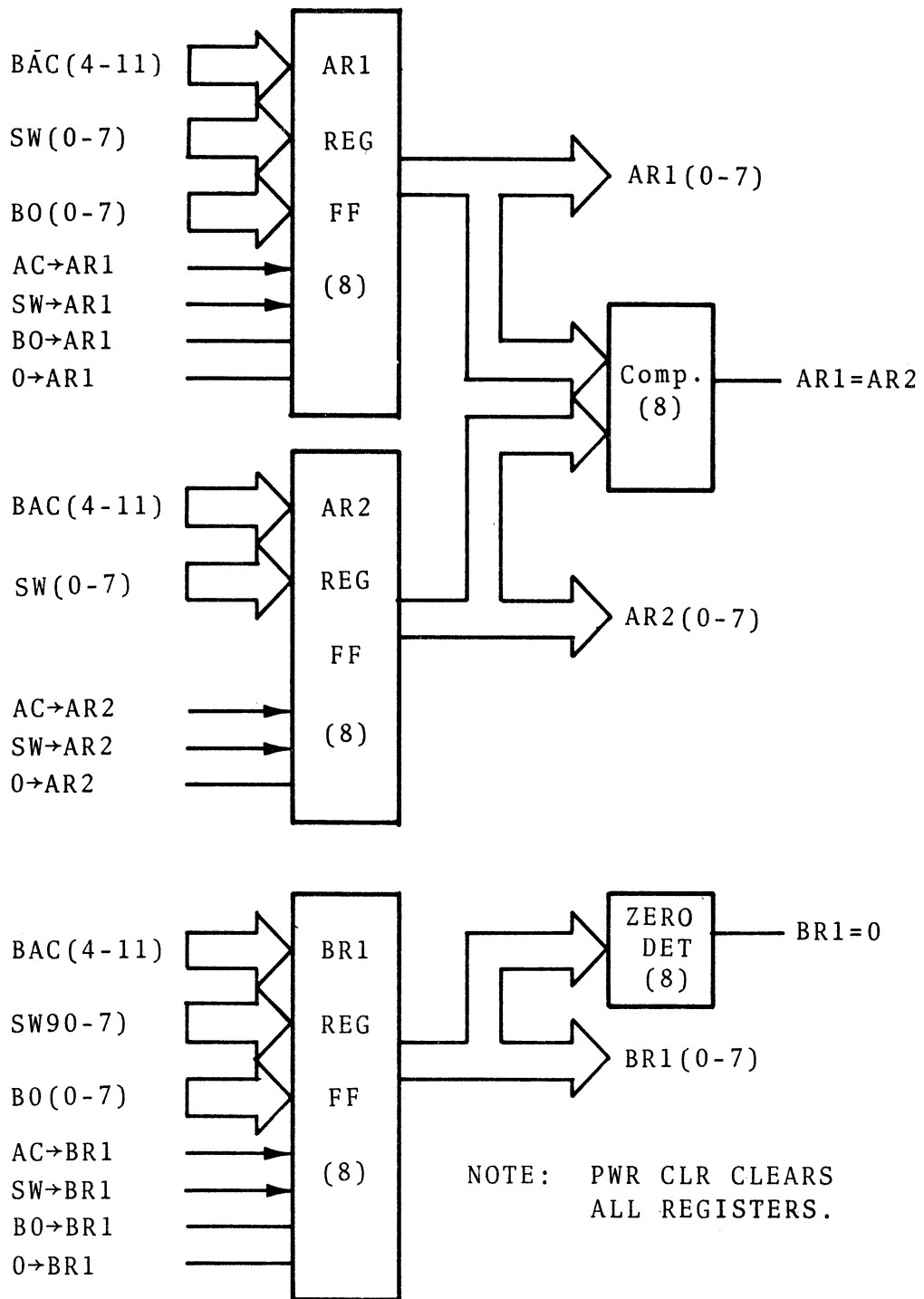
FIGURE 10a.   AR1, BR1, AR2 REGISTERS.
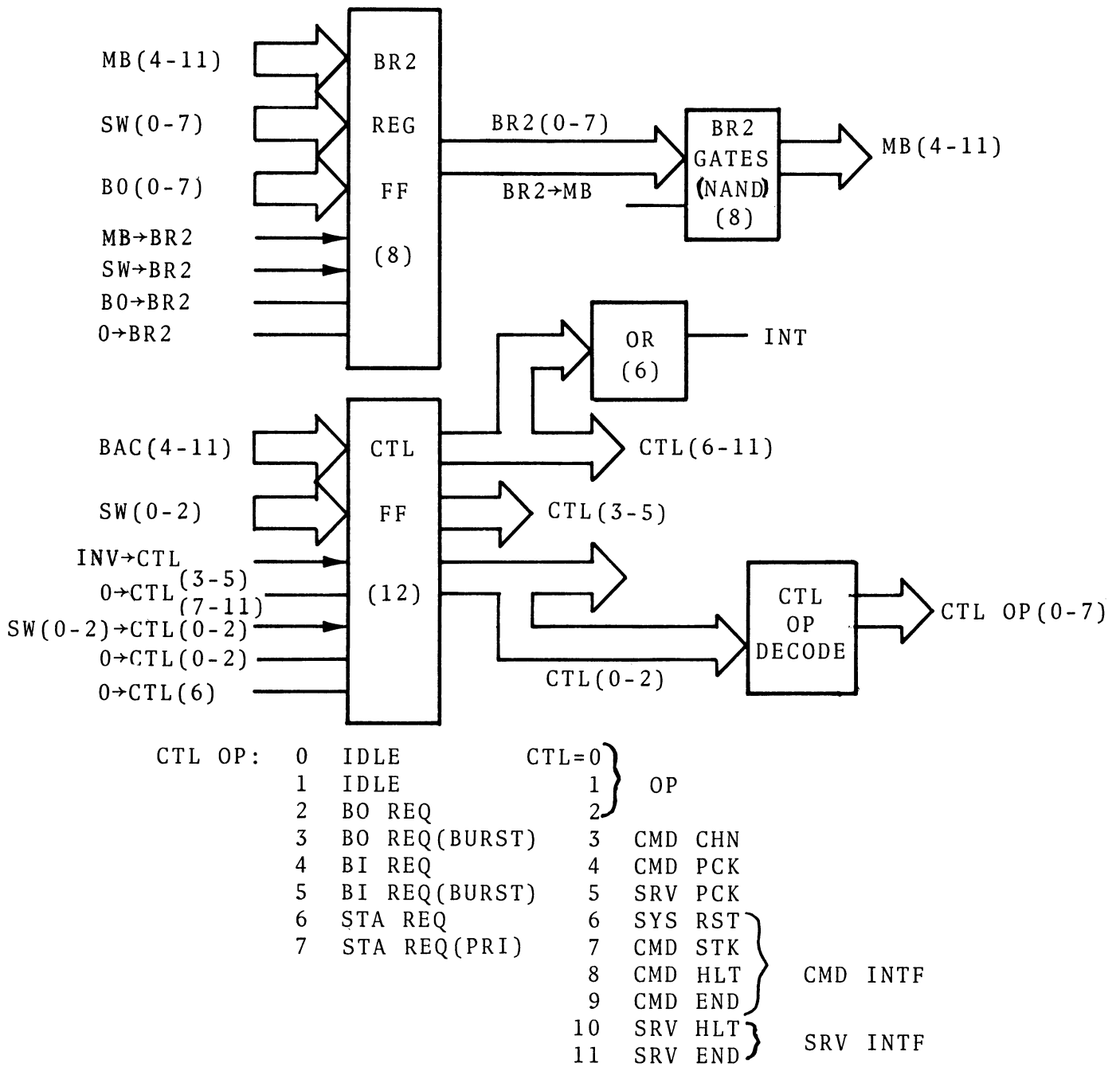
FIGURE 10b. BR2 AND CTL REGISTERS
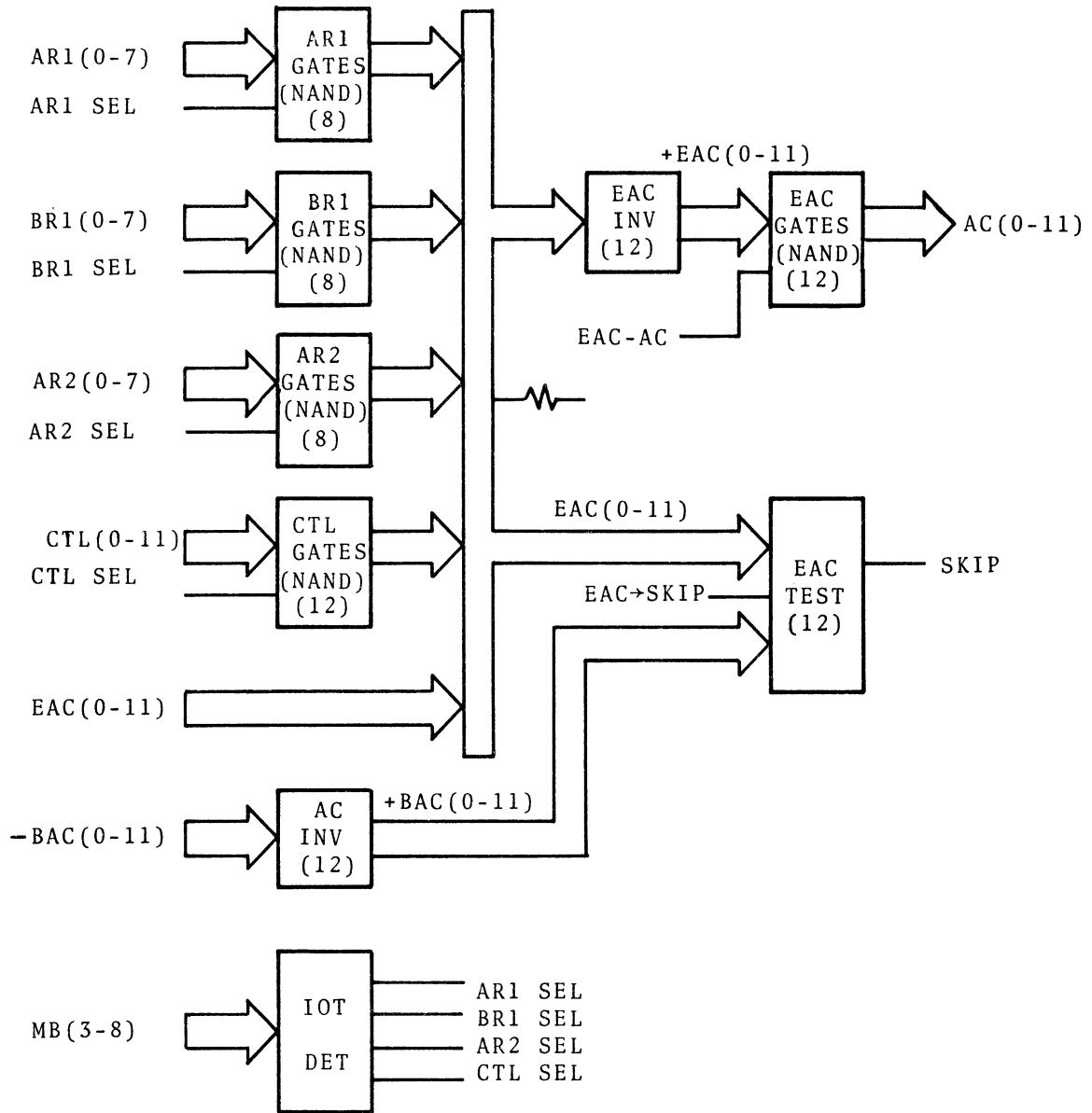
FIGURE 11.   PDP-8 DATA PATHS
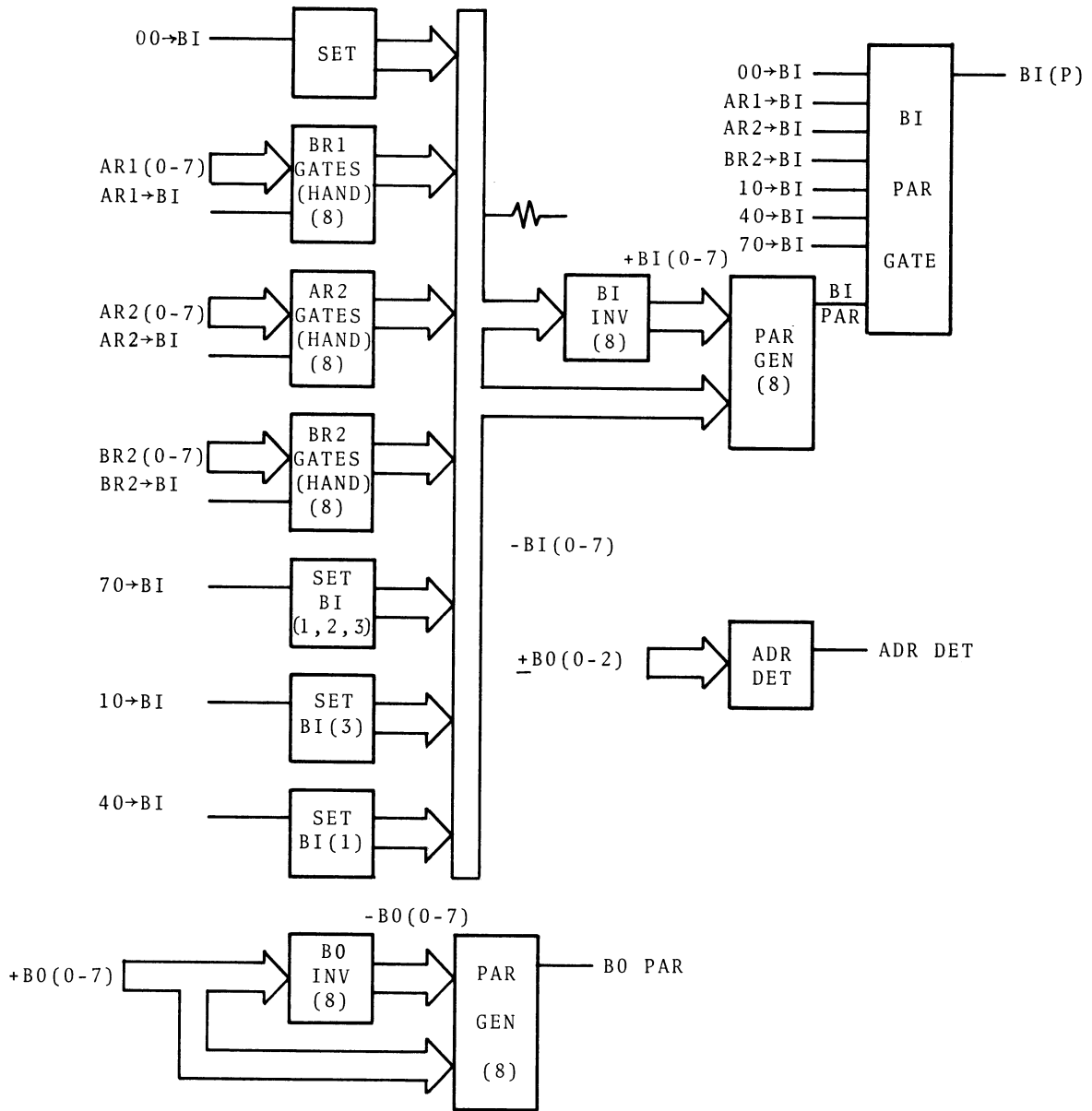
FIGURE 12. BUS GATING

central to the operation of the interface and is discussed
below.

Figures 13 and 14 show respectively the logical
organization of the circuitry used to intercept polling
signals from the channel and that used to seize the control
unit interface for the various kinds of sequences. During an
initial selection sequence, the OUR ADR gate (Figure 13)
detects the conditions for channel-requested service (initial
selection) and the REQ IN gate detects the condition for
control-unit requested service (service cycle). These gates
may not respond simultaneously.

The remaining circuitry shown in Figure 13 is used
in conjunction with the channel polling signal to detect the
conditions under which the interface may seize the channel.
The principal functional block in this circuitry is the
select latch, shown in simplified form in Figure 13 but
actually consisting of two interconnected flip-flops. This
rather interesting circuit is a high-speed two-input switch
with inputs derived from SEL OUT and from the two service-
request gates OUR ADR and REQ IN. An analysis of this circuit
is given in Appendix C .

When SEL OUT rises at the interface while either of
the two service-request gates OUR ADR and REQ IN have true-
valued outputs, the interface will fall into one of three
states: CMD CYC, SRV CYC, or CU BUSY (see Figure 14). If
OUR ADR is true and if the command interface is not busy
(i.e., contains no previously stored command), then CMD INT
is false and CMD CYC state is entered; if OUR ADR is true
and if the interface is busy, then CMD INT is true and the
CU BUSY state is entered. If OUR ADR is false and if REQ IN
is true, then the SRV CYC state is entered. Entrance into
either the CMD CYC or the SRV CYC state causes OPL IN to be
raised after a short delay to allow the circuitry to stabi-
lize, and entrance into the CMD CYC state causes the address
presented by the channel on BUS OUT to be jam-transferred to
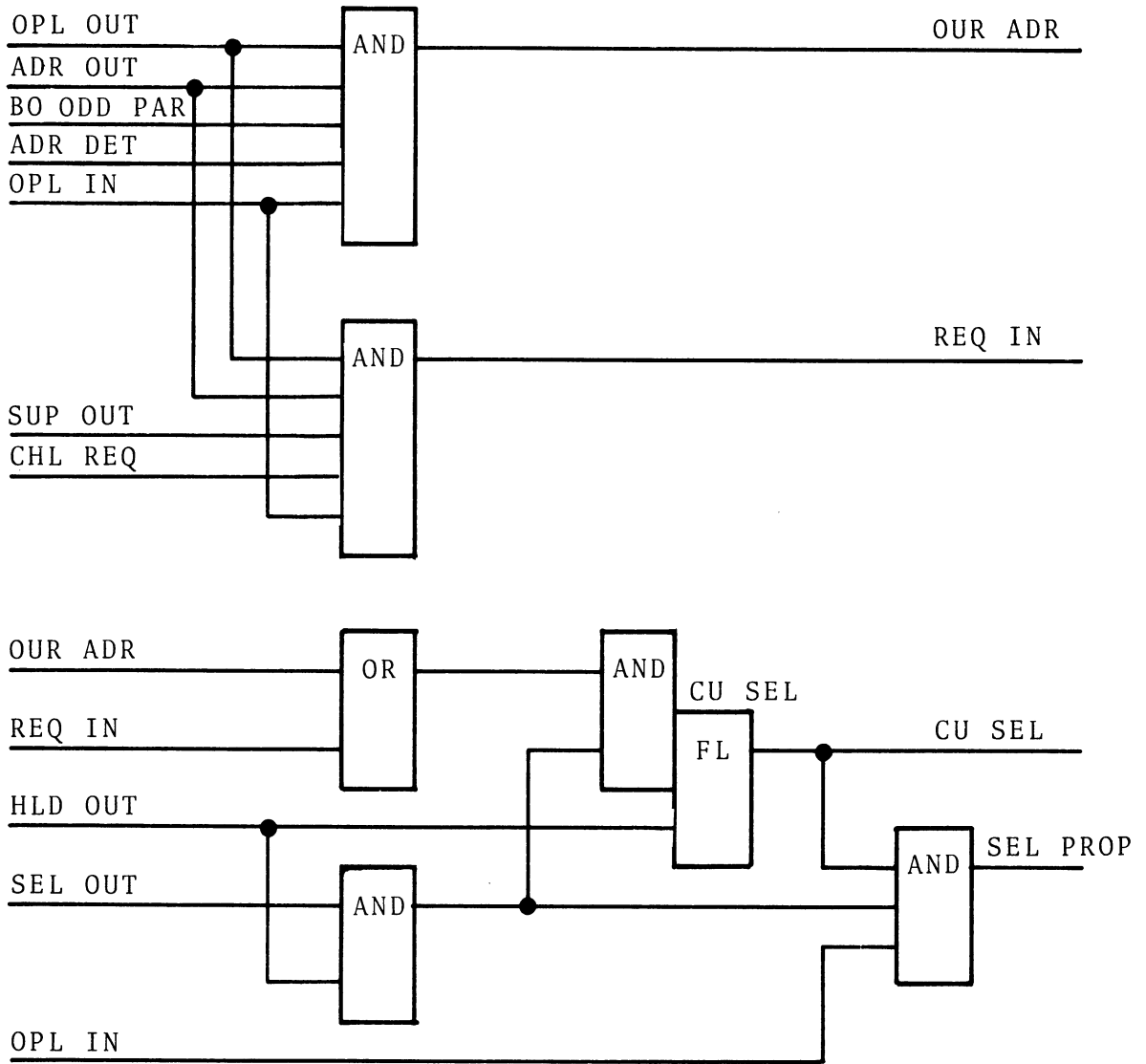
FIGURE 13. SELECT INTERCEPTION
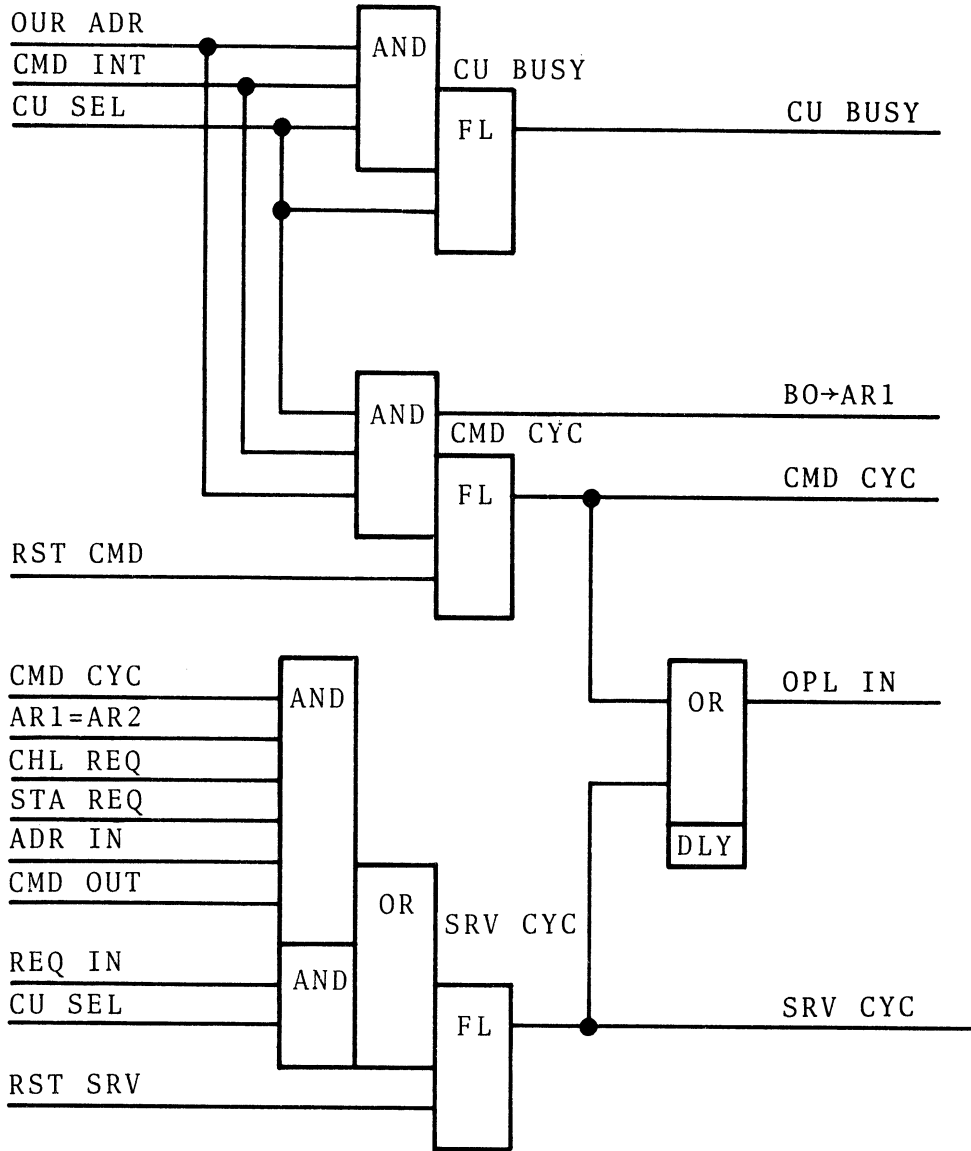
FIGURE 14.   CHANNEL SEIZURE.

AR1. Entrance into the CU BUSY state causes the control-unit-busy byte to be placed on BUS IN, and STA IN to be raised without disturbing any of the active interface registers. The CMD CYC and SRV CYC flip-flops each have their own reset line, which is connected to gates described below. The CU BUSY flip-flop is reset when SEL OUT drops.

Figure 15 shows the logical organization for the circuitry used during the command-storage/proceed phases of the sequences initiated by entrance into either the CMD CYC and SRV CYC states. Both of these sequences begin by placing on BUS IN the contents of AR1 or AR2 as appropriate and proceeding through the channel sequence until CMD OUT is dropped. During the CMD CYC sequence the byte on BUS OUT is transferred to BR1 when CMD OUT is raised by the channel. The short delays indicated on Figure 15 allow time for the parity circuitry to stabilize before bus transfers are executed.

Following the command-storage/proceed phase of either the CMD CYC or SRV CYC sequence, both the CMD DLY and CHL SRV flip-flops are set. These flip-flops are reset when OPL IN drops. When the CHL SRV flip-flop becomes set, a byte of data or status information may be transferred between the channel and the interface. If the CMD CYC flip-flop is set, then the sequence ends by presenting to the channel either an all-zero status byte or a status byte containing the status modifier bit, depending upon whether BR1 has been stored as a nonzero byte or a zero byte respectively. If the SRV CYC flip-flop is set, then the sequence ends by transferring a byte from BUS OUT to BR2 (channel-outbound service requested) or from BR2 to BUS IN (channel-inbound data or status service requested) with the appropriate tag line. If the CU BUSY flip-flop is set, then a status byte containing the status modifier, control unit end, and busy bits is placed on BUS IN. Appropriate delays are included to allow time for the parity circuitry to stabilize and for skew distortion to stabilize. Outbound parity-checking circuitry is shown in Figure 17.
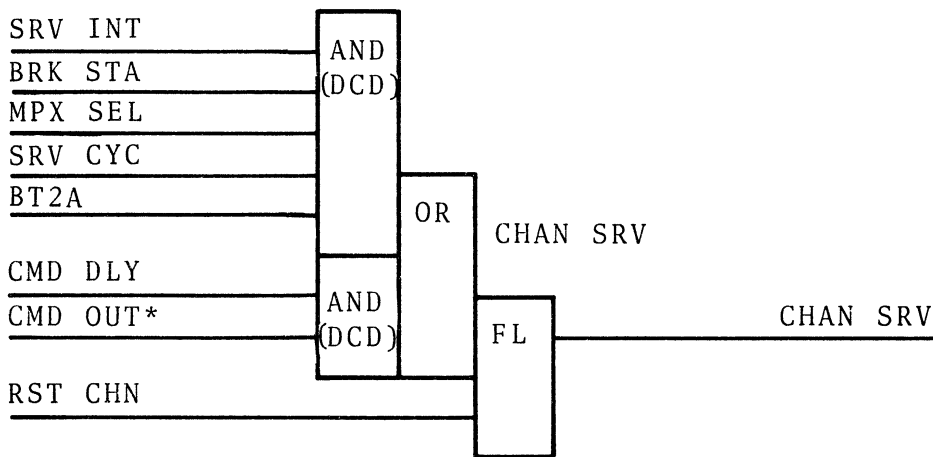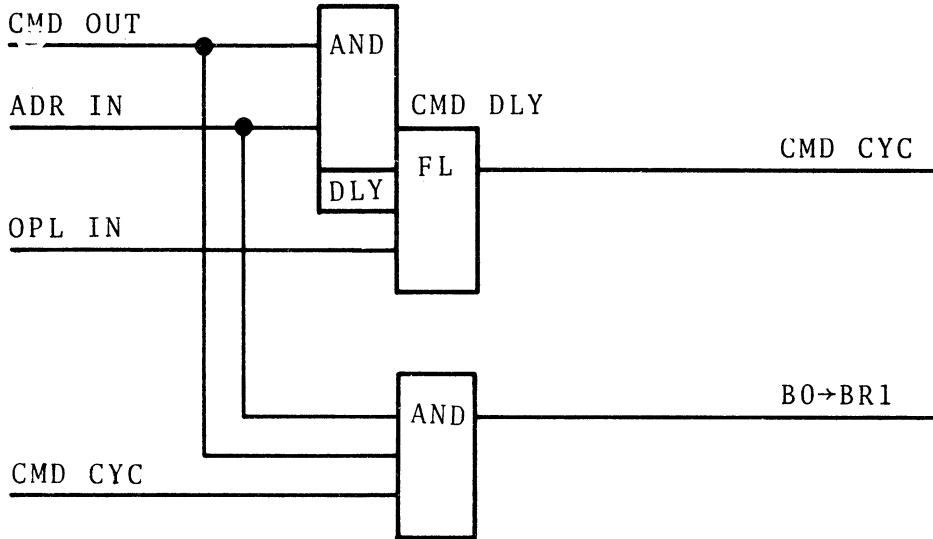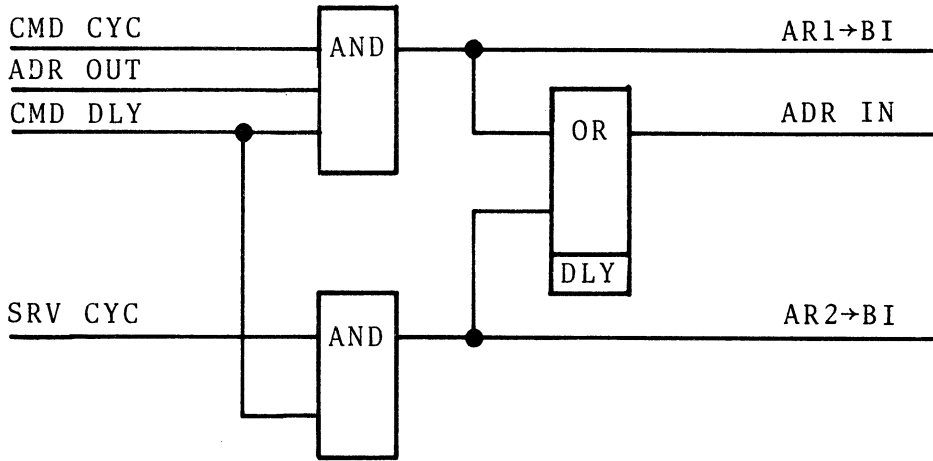
*DROP TRANSITION

FIGURE 15.   COMMAND STORAGE/PROCEED
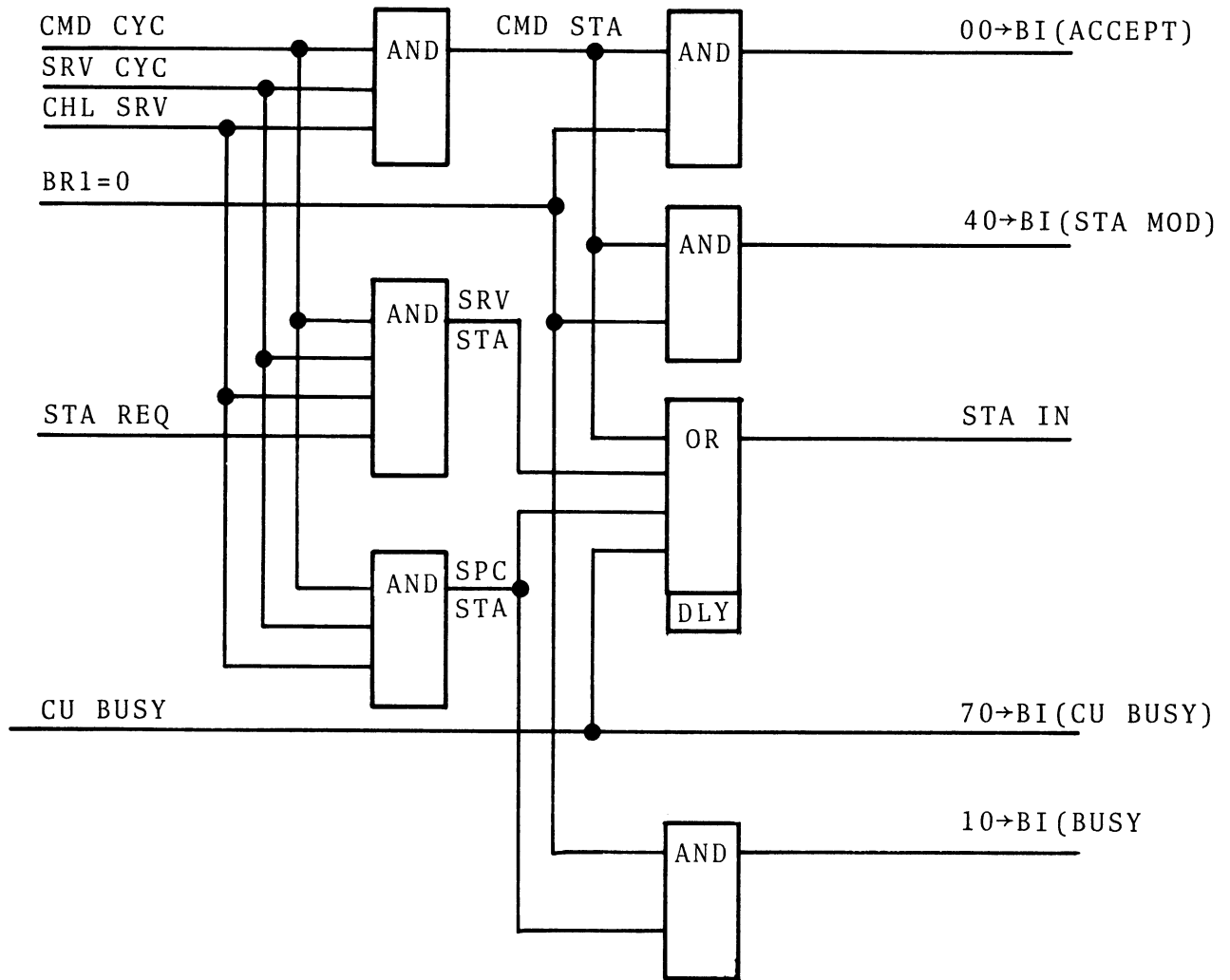
FIGURE 16.   STATUS
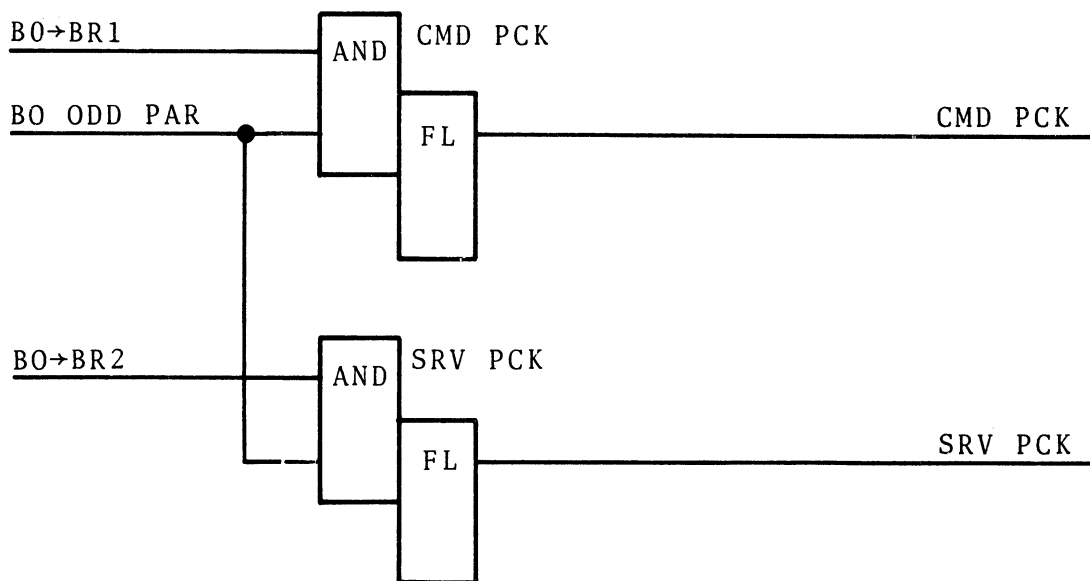
FIGURE 17. PARITY CHECK

If a status request is pending at the time an initial selection procedure is signalled by the channel, then, if the contents of AR1 match those of AR2, the SRV CYC flip-flop will be set when the channel command is stored in BR2. (See gate next to SRV CYC flip-flop in Figure 14.) This special condition is detected when the status byte is transmitted to the channel. If both CMD CYC and SRV CYC flip-flops are set following the command—storage/proceed phase of the sequence, then BR2 is transferred to BUS IN and STA IN is raised. If, furthermore, the command byte stored in BR1 during the sequence contains nonzero bits, then the busy bit is logically OR'ed into the status byte. Figure 18 shows the details of the BR2 gating.

The terminating conditions for the CMD CYC sequence are shown in Figure 19. If a nonzero command byte has been stored in BR1 during a CMD CYC sequence, and if the channel has responded to presentation of the all-zero status byte with SRV OUT (any other response is an equipment check), then the CMD END bit is set in the control register. If an all-zero command byte has been stored in BR1 during the sequence and if the channel has responded to the presentation of the status byte containing the status modifier bit with CMD OUT (stack status on initial selection), then the CMD STK bit is set in the control register. These are the only two bits that can be set following a complete CMD CYC sequence, and they are mutually exclusive.

If at any time, either during an interface operation or not, both SUP OUT and OPL OUT are down at the interface, the CMD RST bit is set in the control register. This operation clears all control register bits except the CMD RST bit, which is forced to the set condition, and in addition clears all flip-flops in the interface to the channel-disconnect condition. If during a CMD CYC sequence ADR OUT is up at the interface while SEL OUT is down (interface disconnect) or SUP OUT is up while OPL OUT is down (selective reset), then the CMD HLT
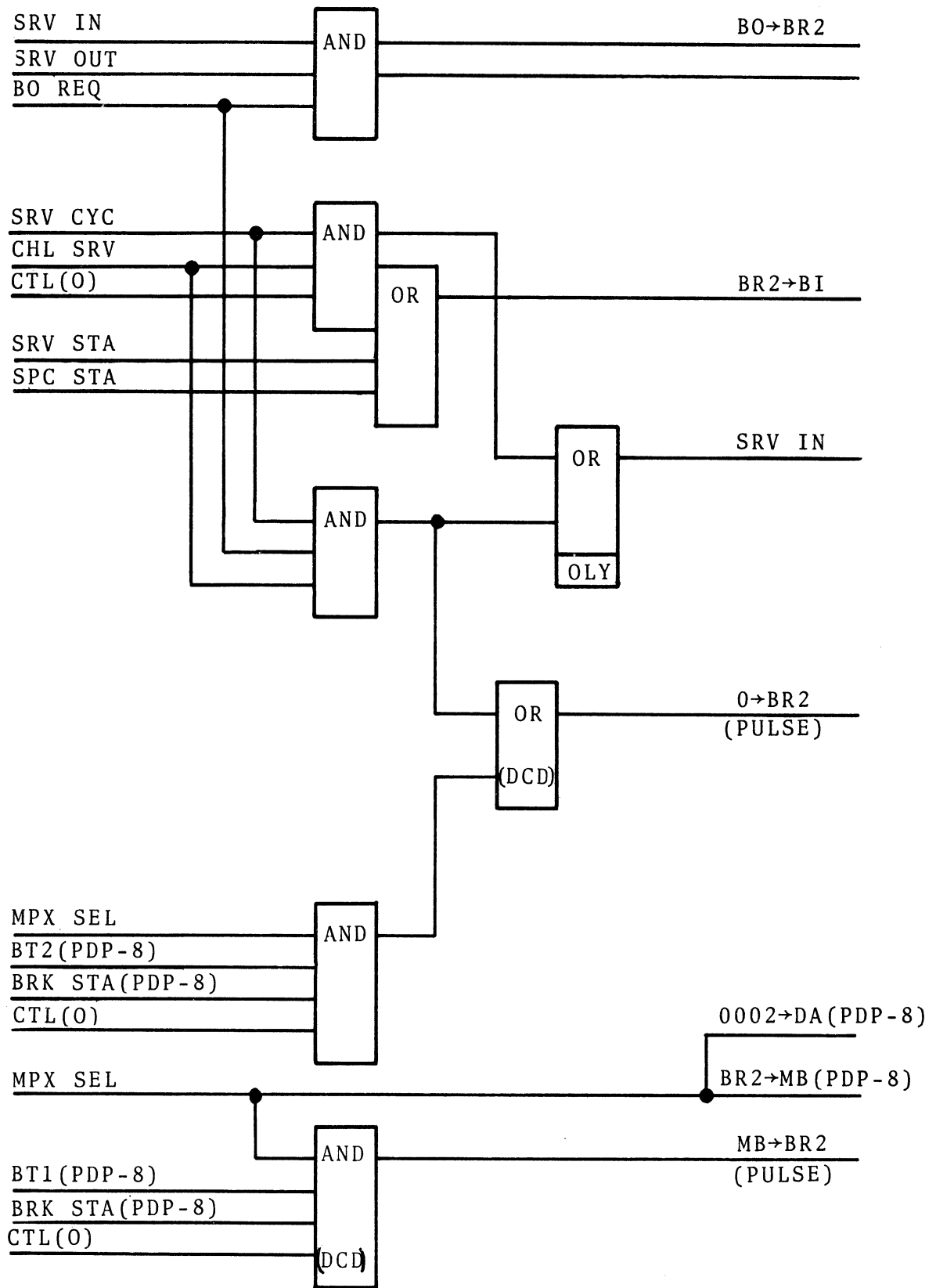
FIGURE 18. BR2 GATING
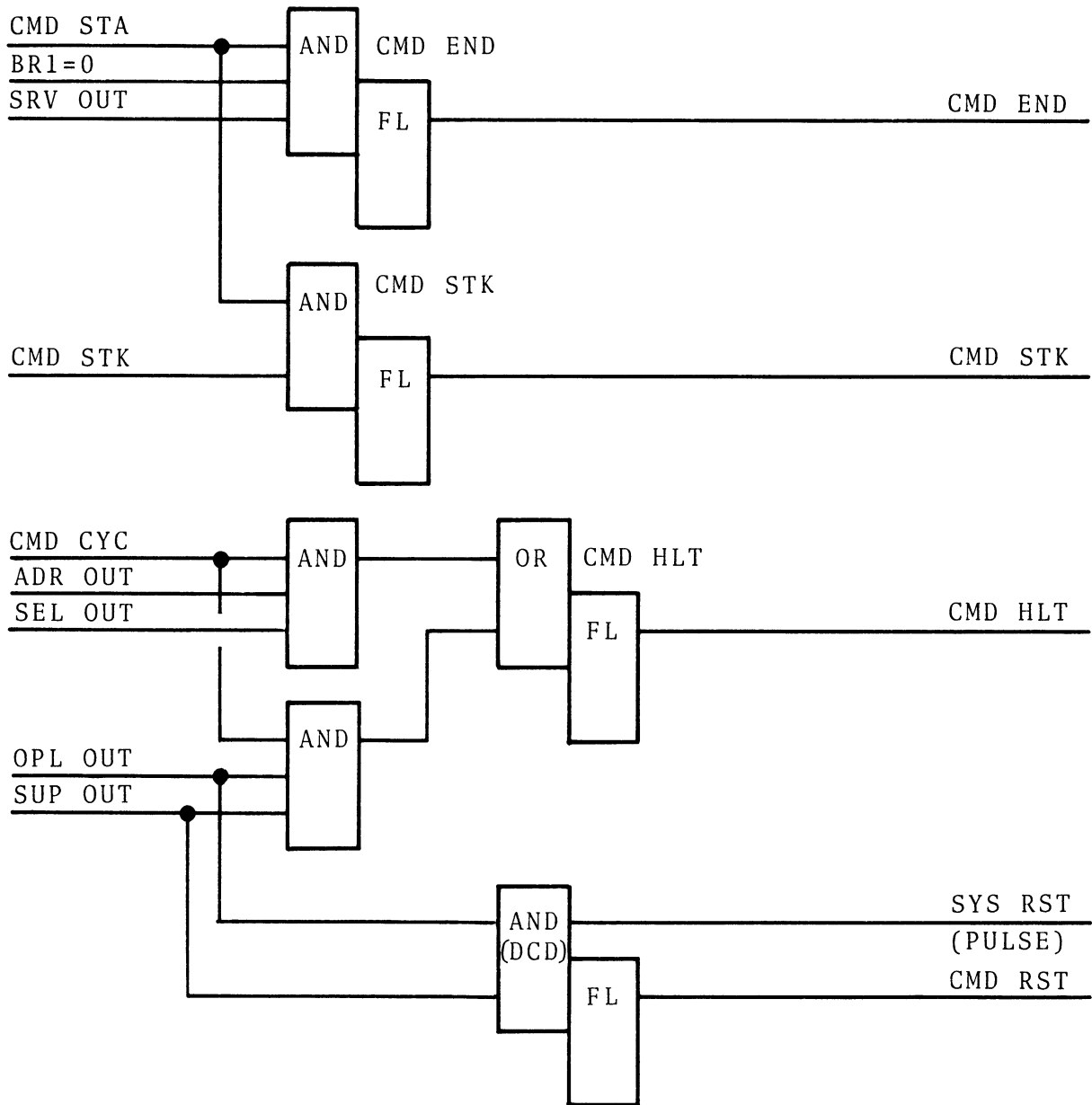
FIGURE 19. COMMAND END

bit of the control register is set. This operation clears all flip-flops in the interface to the channel-disconnect condition.

The terminating conditions for the SRV CYC sequence are shown in Figure 20. This sequence may end in three ways:

        a. in a request for a data break operation to fetch a data or status byte from PDP-8 core memory (BRK REQ),

        b. in an ending condition which stops data transmission and interrupts the PDP-8 program (SRV END and SRV HLT), or

        c. in a stack-status condition which disconnects the interface from the channel and immediately re-requests channel service.

The PREP END flip-flop is set on a data or status operation in which the PDP-8 block transfer word count decrements to zero. In the channel-inbound case the channel must either accept or reject the byte before an ending-condition bit (SRV END or SRV HLT) is set in the control register.

Following the ending operation in the case either of a CMD CYC or SRV CYC sequence, the interface is disconnected from the channel with the circuit shown in Figure 21. Here the various terminating conditions are detected and the reset signals for the CMD CYC and SRV CYC flip-flops are generated. In addition, signals are derived that condition the PDP-8 interrupt bus (INT REQ) and that indicate that the command interface is busy (CMD INT).

The channel-request circuitry is shown in Figure 22. Note that when a channel-outbound request is initiated a special pulse is generated which sets the CHL REQ flip-flop and starts the operation. Conversely, when a channel-inbound data or status request is initiated a special pulse is generated which sets the BRK REQ flip-flop (see Figure 20) and starts the operation.
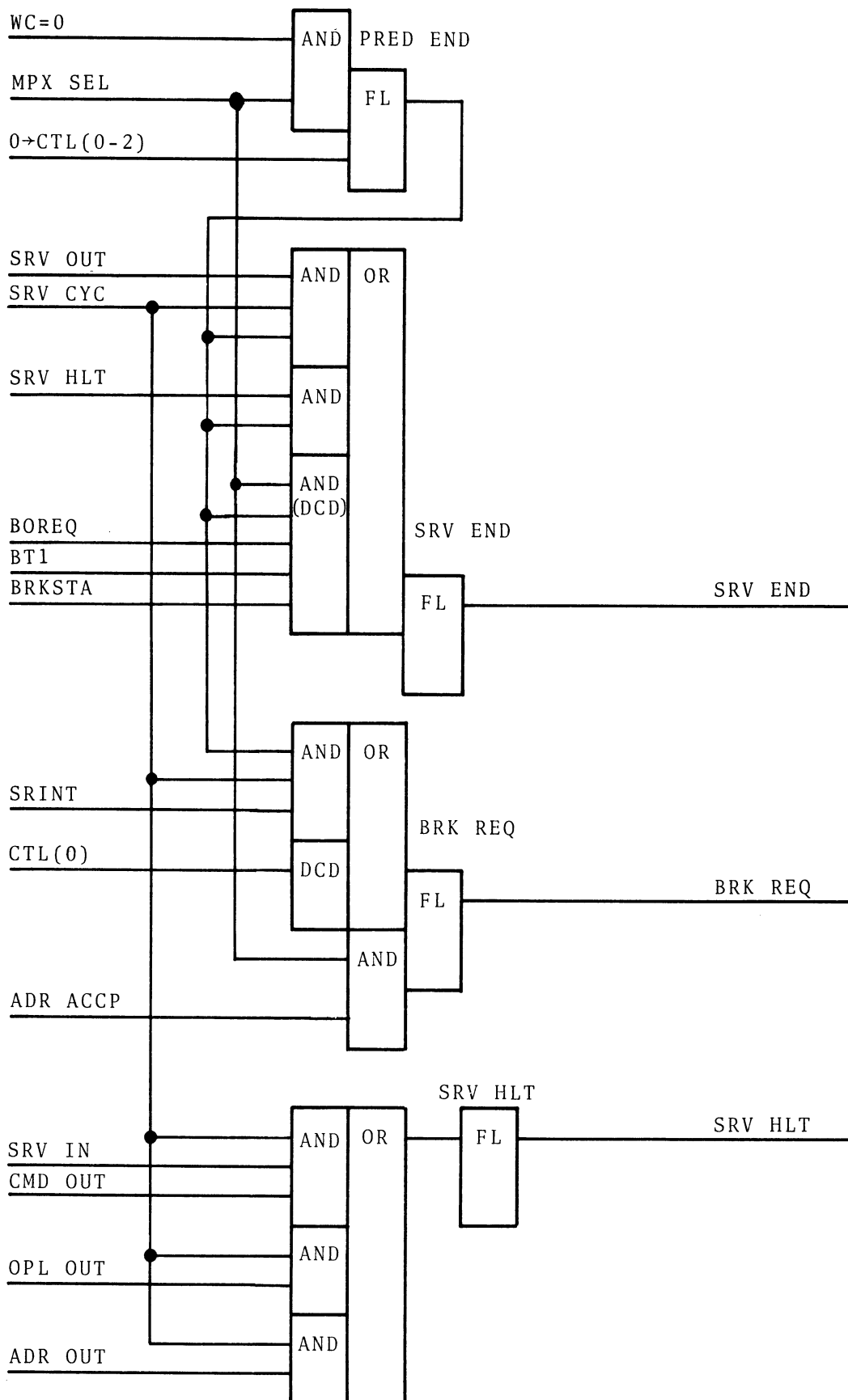
FIGURE 20. SERVICE END
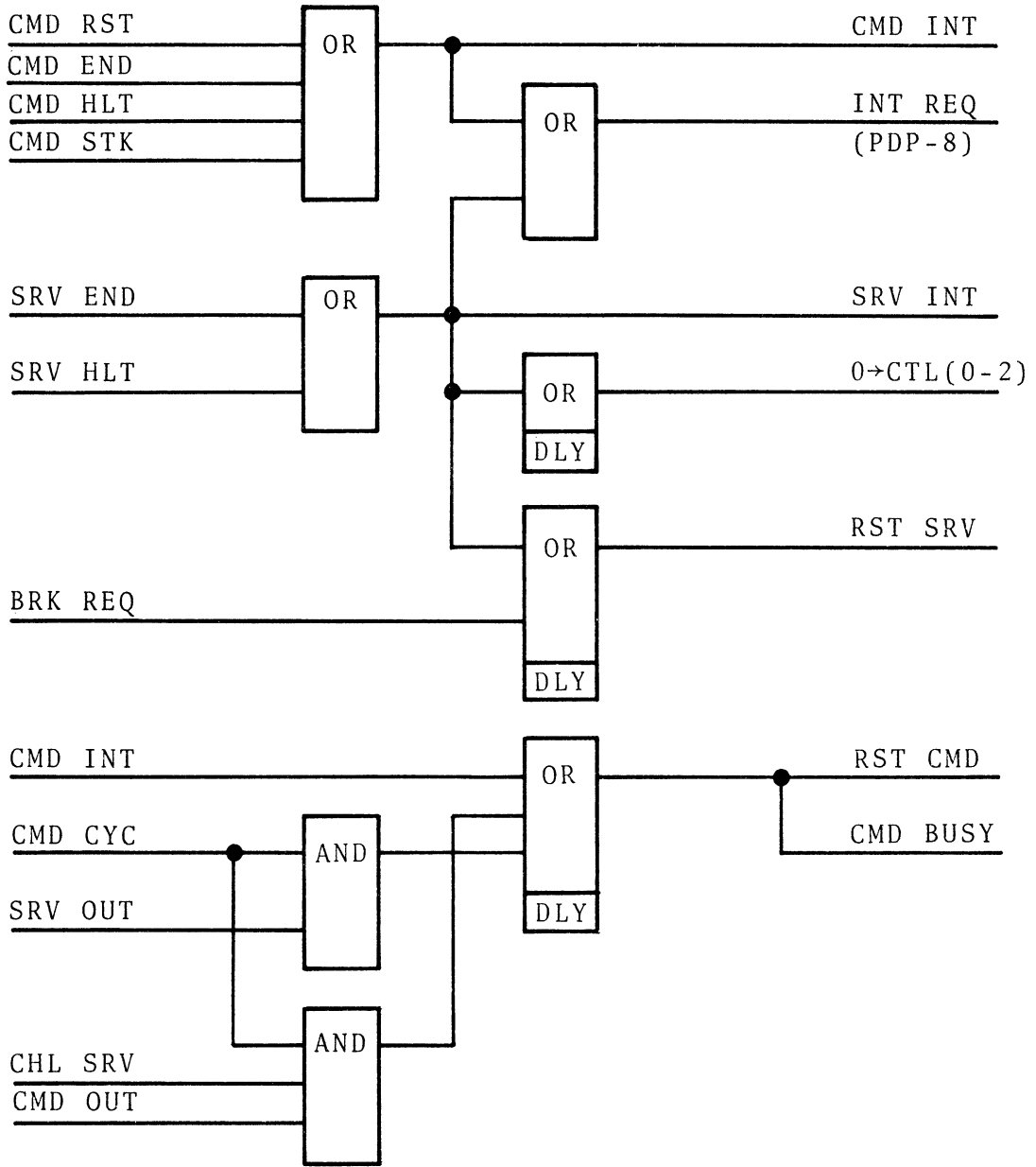
FIGURE 21. CYCLE RESET
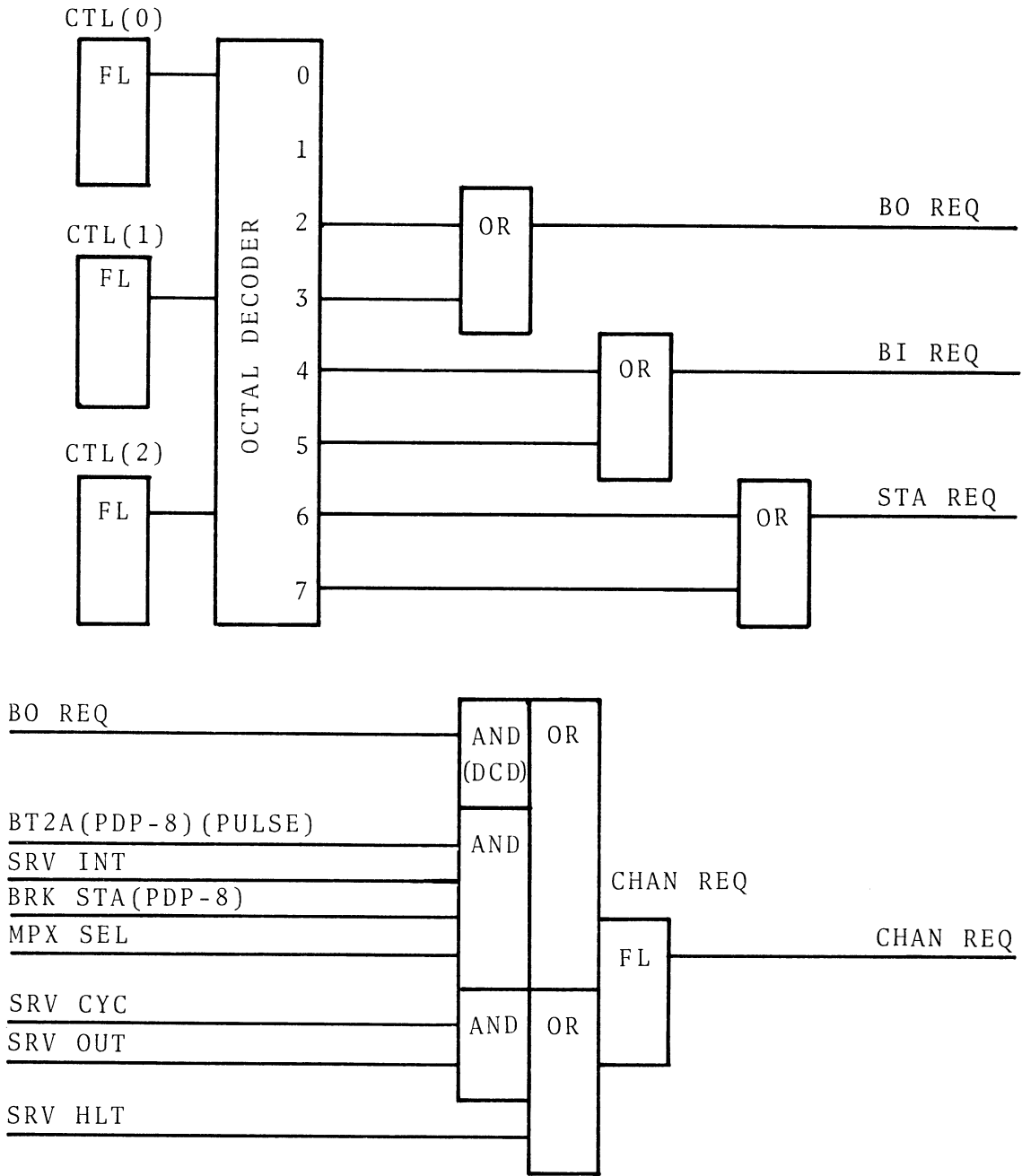
FIGURE 22. CONTROL OPERATION DECODER AND CHANNEL REQUEST
FLIP-FLOP.

Additional details of interface operation are summarized in flow chart form in Appendix A. Circuit details are shown in Appendix E.

APPENDIX A

CHANNEL SEQUENCE FLOW CHARTS
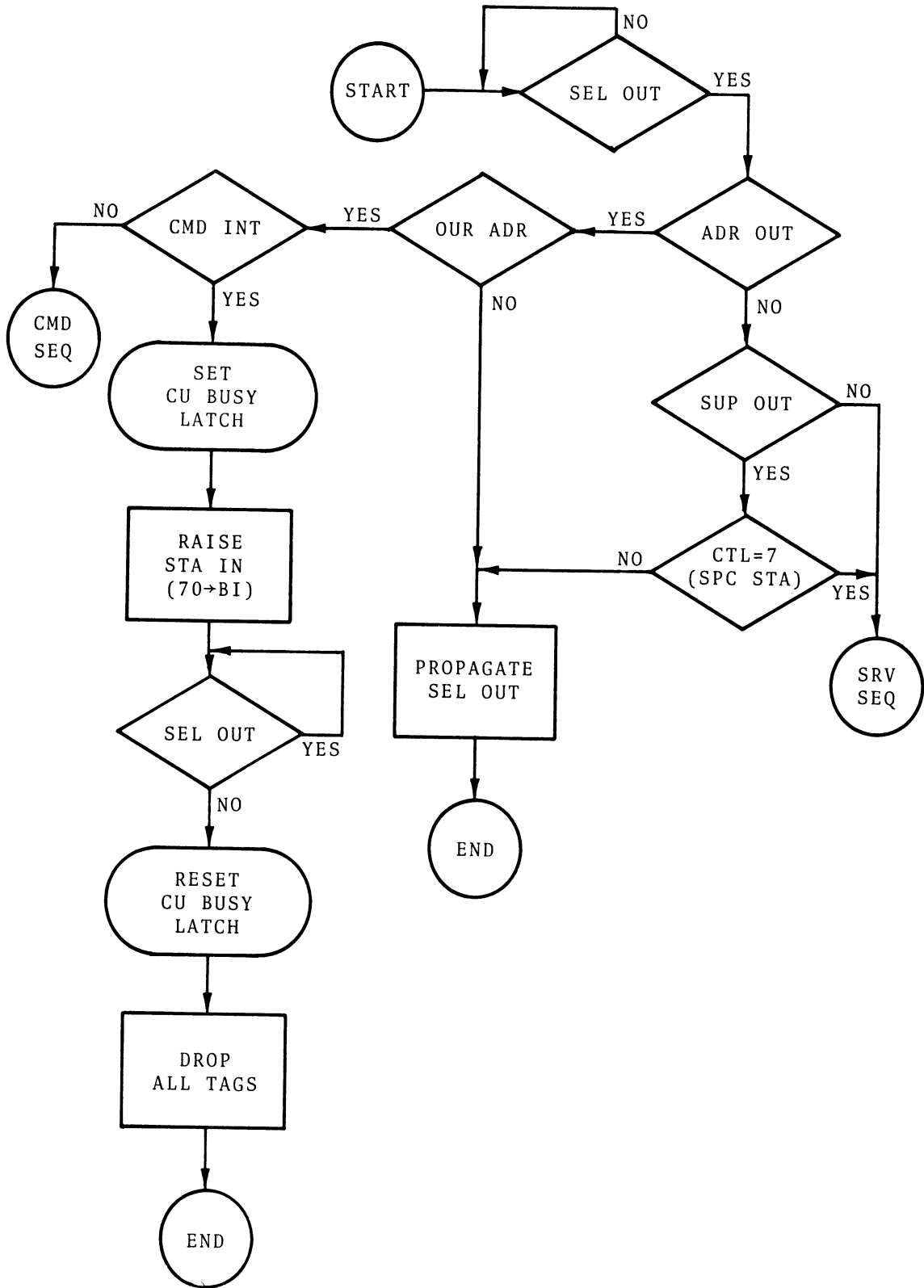
FIGURE A1. CHANNEL SEIZURE
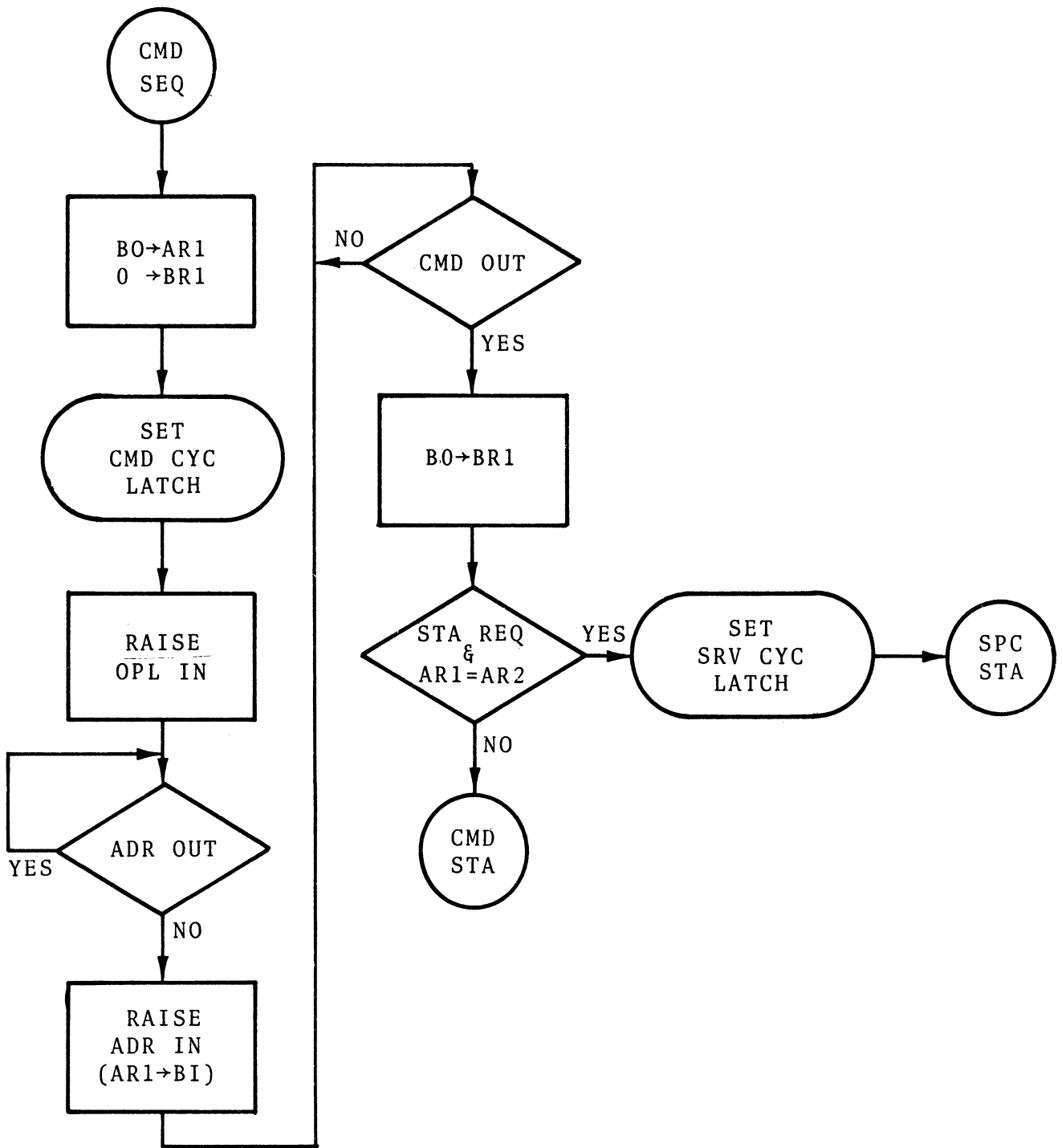
FIGURS A2.   COMMAND BYTE STORAGE
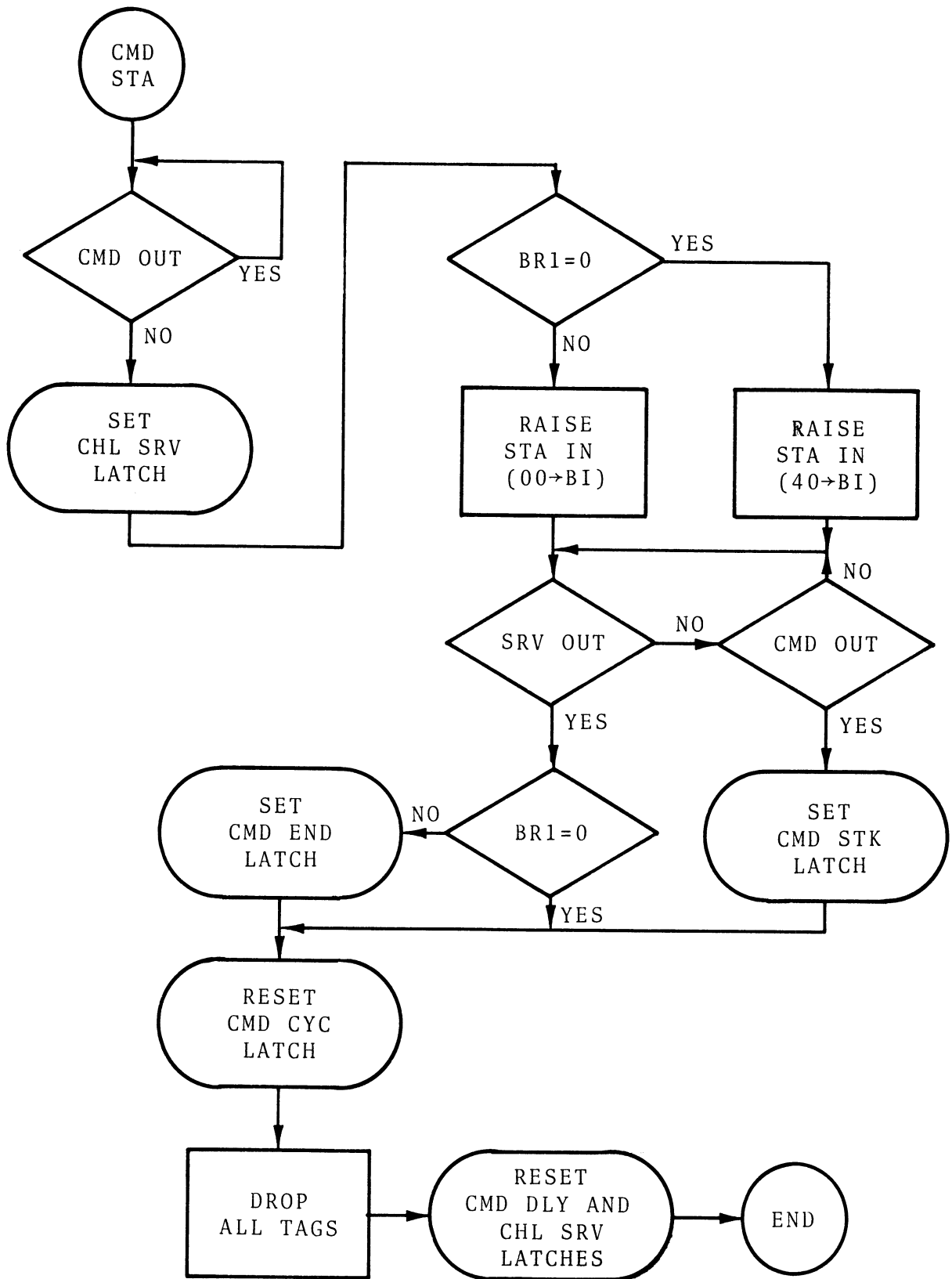
FIGURE A3. COMMAND STATUS PRESENTATION
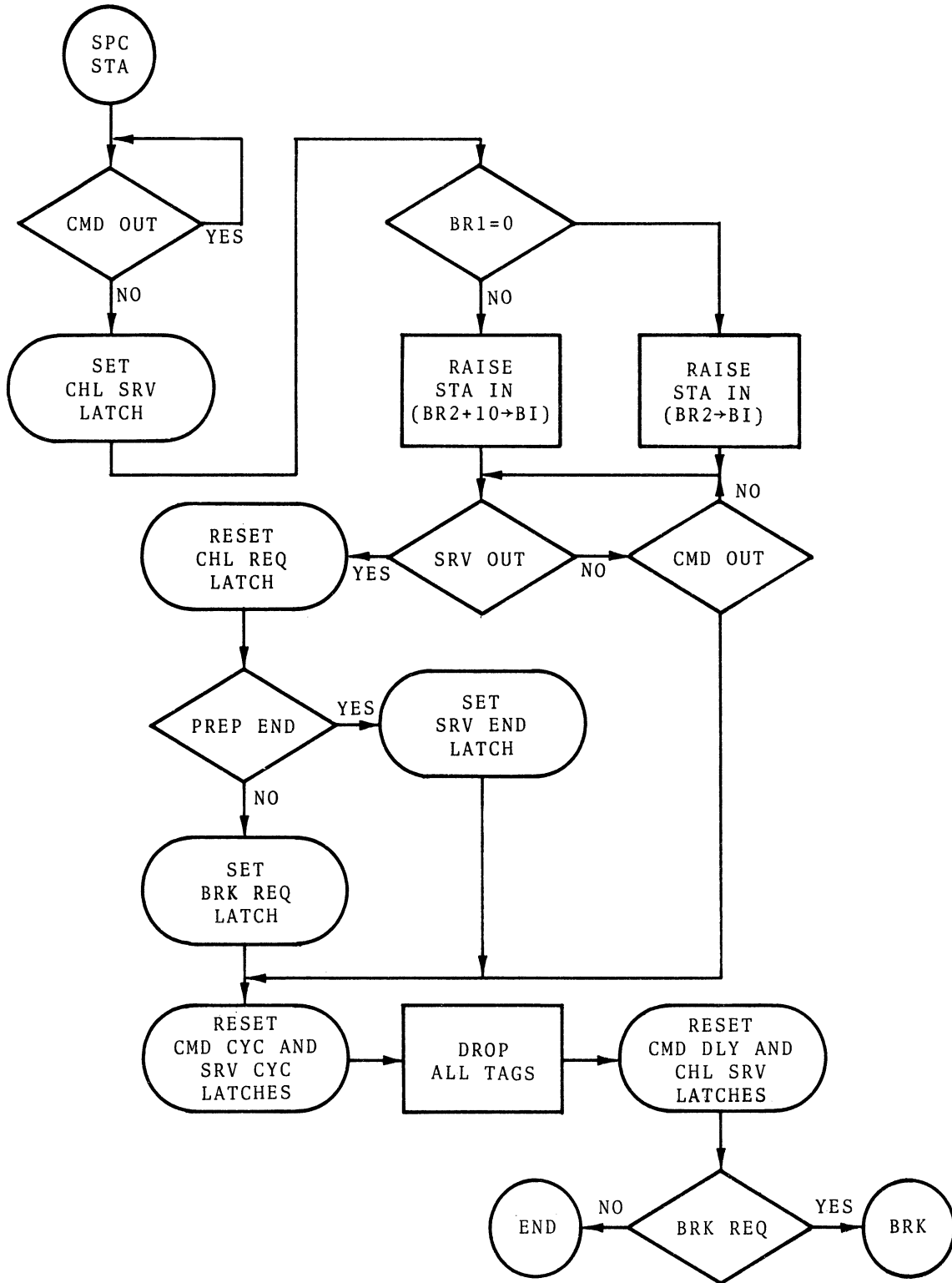
FIGURE A4. SPECIAL STATUS PRESENTATION
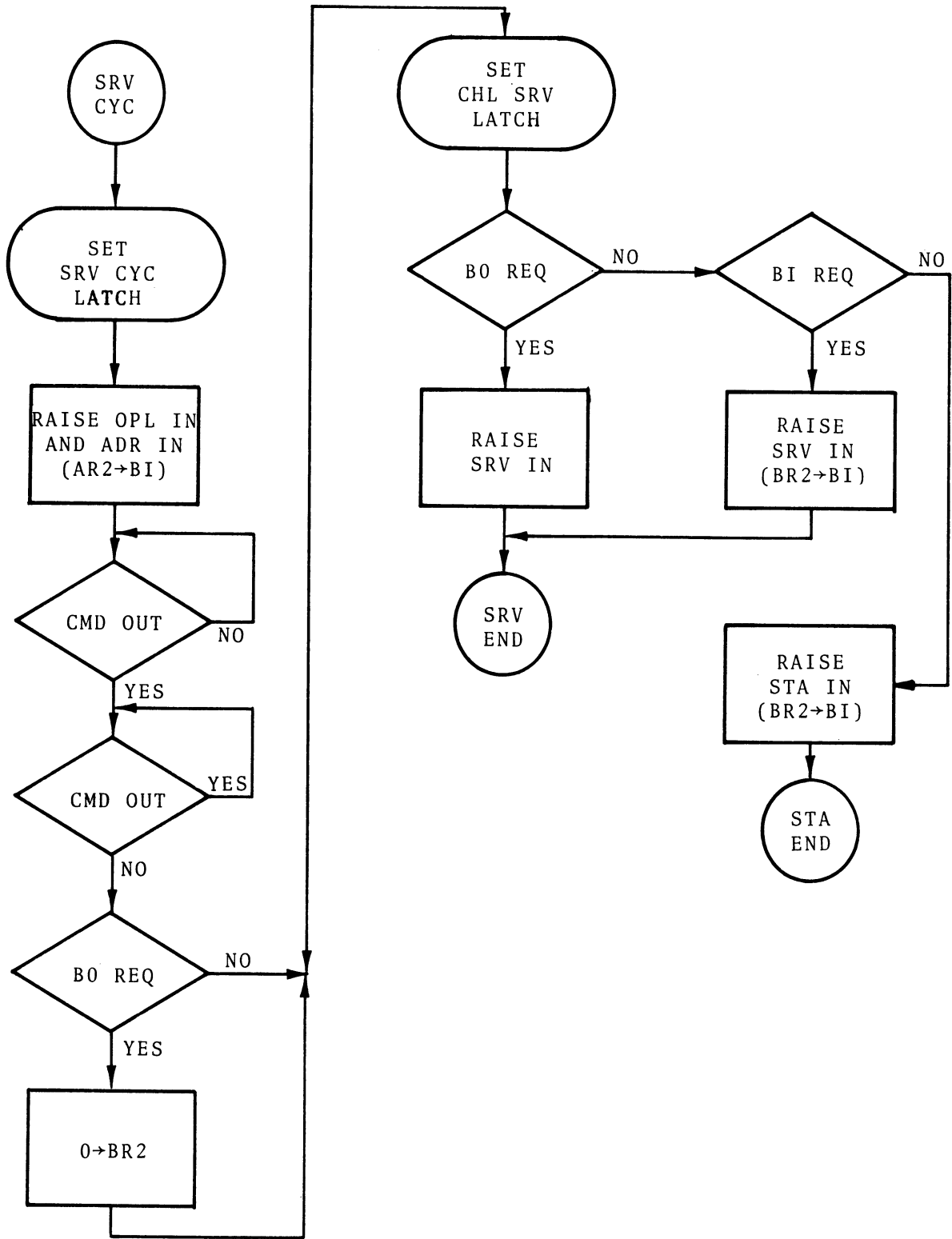
FIGURE A5.   SERVICE CYCLE
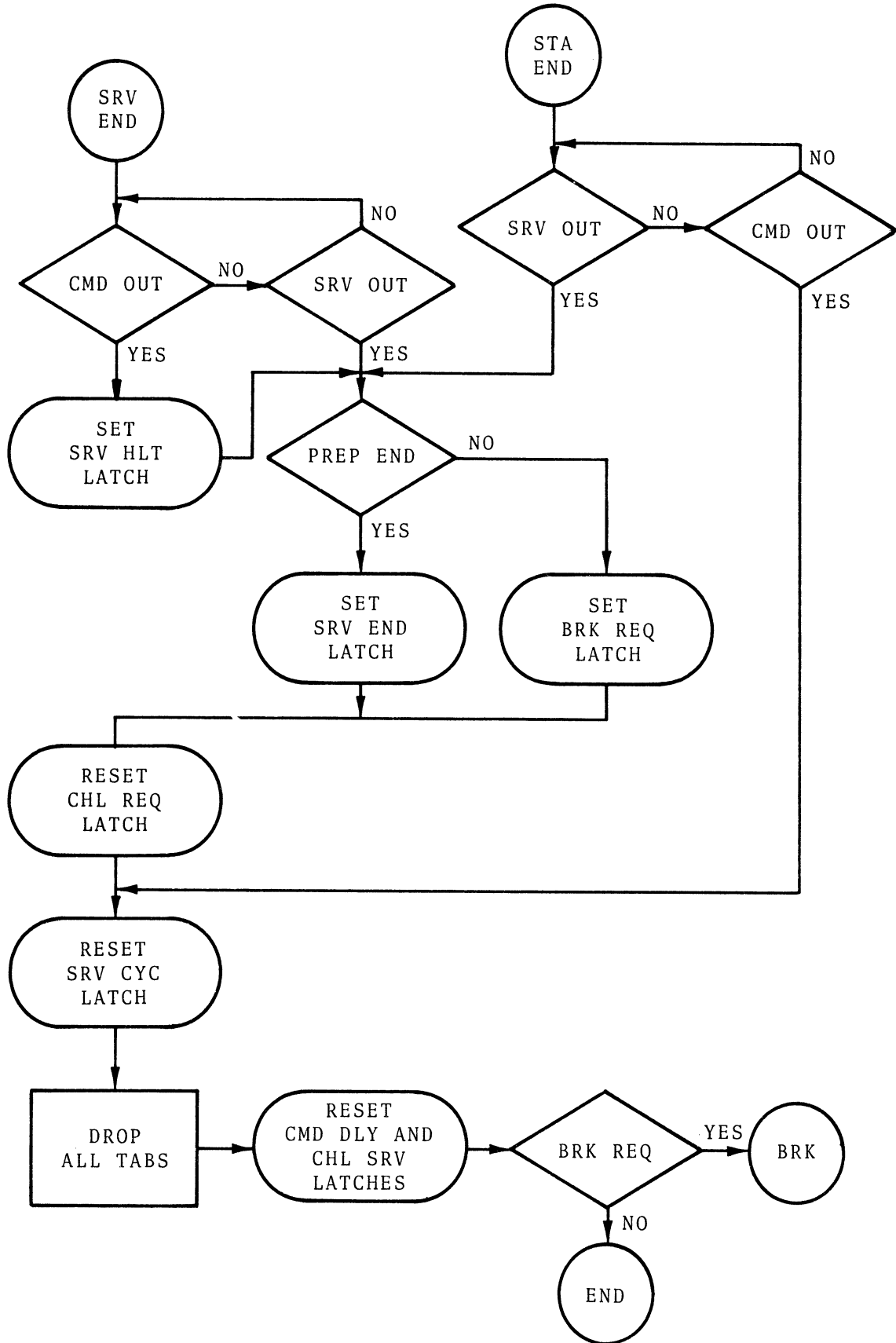
FIGURE A6.   SERVICE CYCLE END
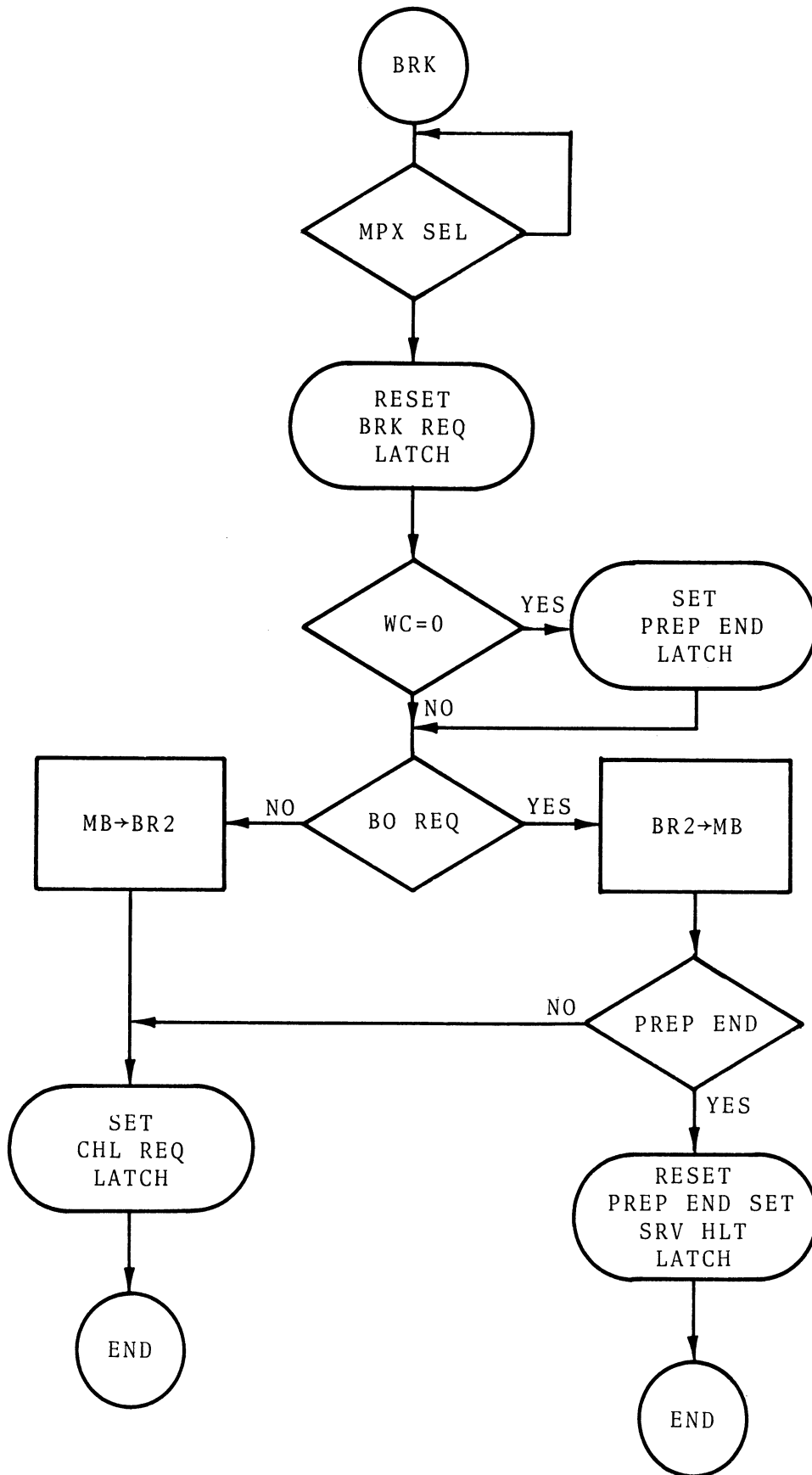
FIGURE A7.   PDP-8 DATA BREAK CYCLE

APPENDIX B

CHANNEL SEQUENCE PHOTOGRAPHS
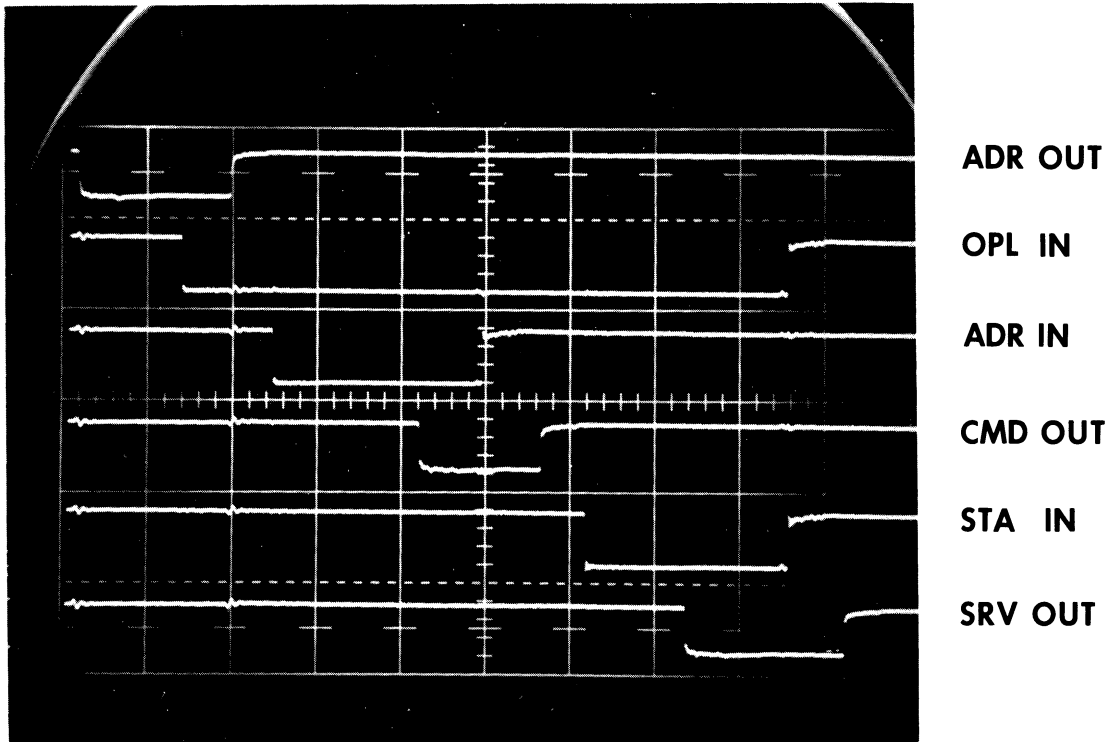
1μS/CM

Fig. B1 INITIAL SELECTION
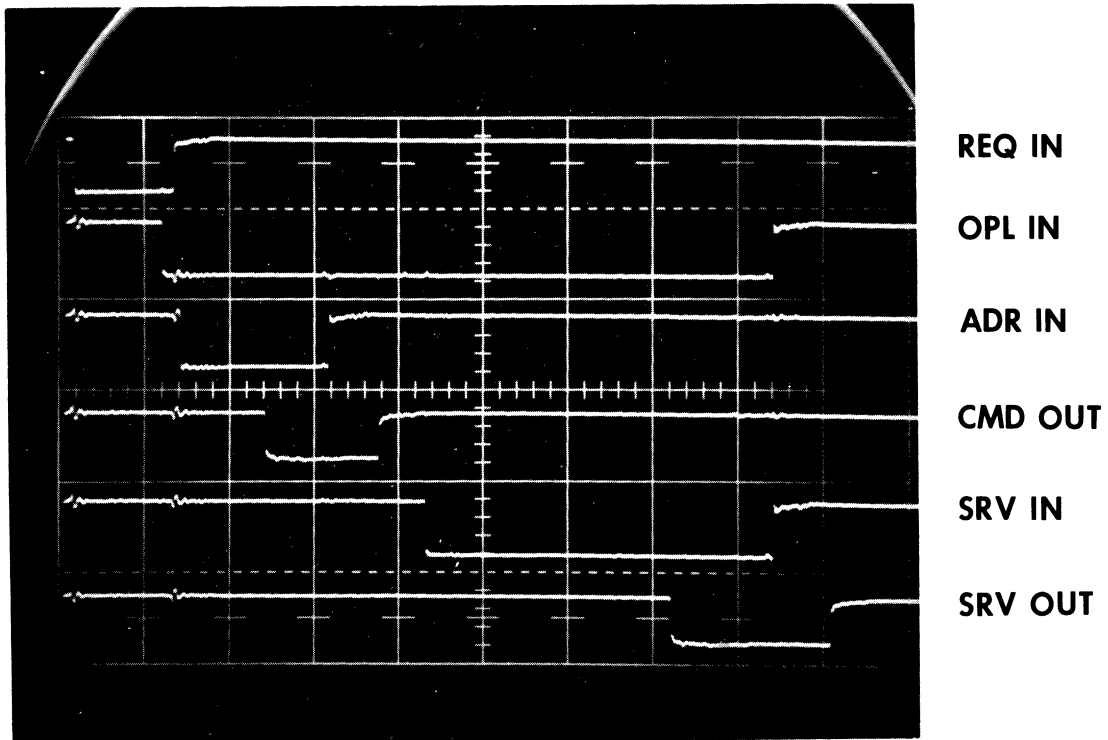
1μS/CM

Fig. B2 SERVICE CYCLE

FIGURE B1

INITIAL SELECTION (1μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	ADR OUT	ADO	1BØ1S	IBM
2	OPL IN	OPI	1BØ1D	IBM
3	ADR IN	ADI	1BØ1H	IBM
4	CMD OUT	CMO	1BØ1T	IBM
5	STA IN	STI	1BØ1E	IBM
6	SRV OUT	SRO	1B31D	IBM

FIGURE B2

SERVICE CYCLE (1μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	REQ IN	REI	1B31M	IBM
2	OPL IN	OPI	1BØ1P	IBM
3	ADR IN	ADI	1BØ1H	IBM
4	CMD OUT	CMO	1BØ1T	IBM
5	SRV IN	SRI	1BØ1K	IBM
6	SRV OUT	SRO	1B31D	IBM

ADR OUT

SEL OUT
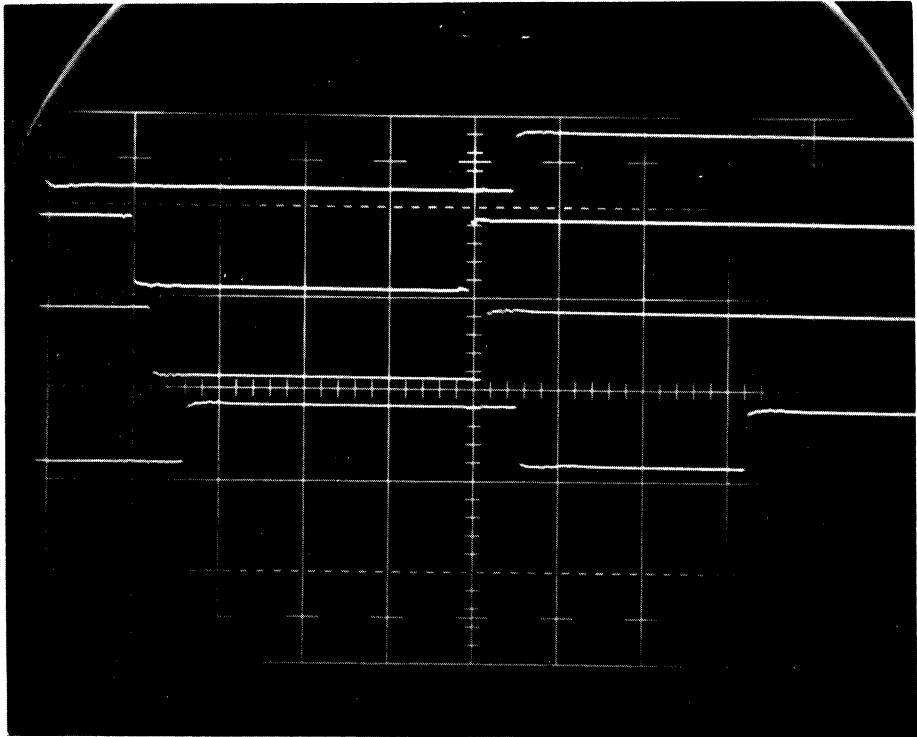
STA IN

SUP OUT

1μS/CM

Fig. B3 CONTROL UNIT BUSY

ADR OUT

SEL OUT

OPL IN

ADR IN
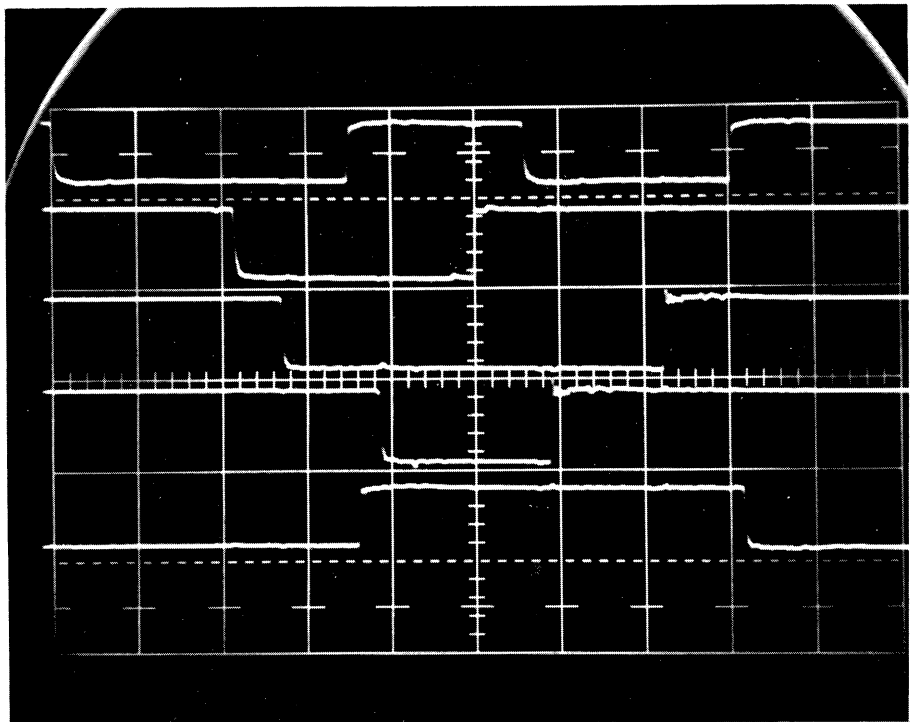
SUP OUT

0.5μS/CM

Fig. B4 INTERFACE DISCONNECT

FIGURE B3

CONTROL UNIT BUSY (1μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	ADR OUT	ADO	1BØ1S	IBM
2	SEL OUT	SEL OUT	1BØ1P	IBM
3	STA IN	STI	1BØ1E	IBM
4	SUP OUT	SUO	1BØ1V	IBM

FIGURE B4

INTERFACE DISCONNECT (0.5μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	ADR OUT	ADO	1BØ1S	IBM
2	SEL OUT	SEL OUT	1BØ1P	IBM
3	OPL IN	OPI	1BØ1D	IBM
4	ADR IN	ADI	1BØ1H	IBM
5	SUP OUT	SUO	1BØ1V	IBM
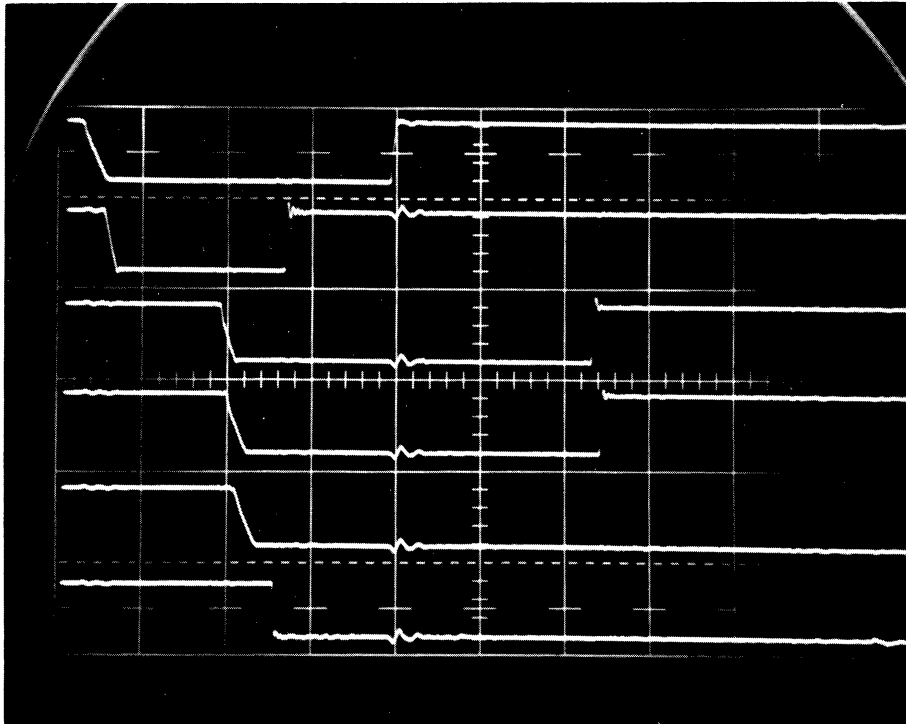
ADR OUT

OUR ADR

SEL OUT

CU SEL

CMD CYC

OPL IN

0.5μ S/CM

Fig. B5 CHANNEL SEIZURE
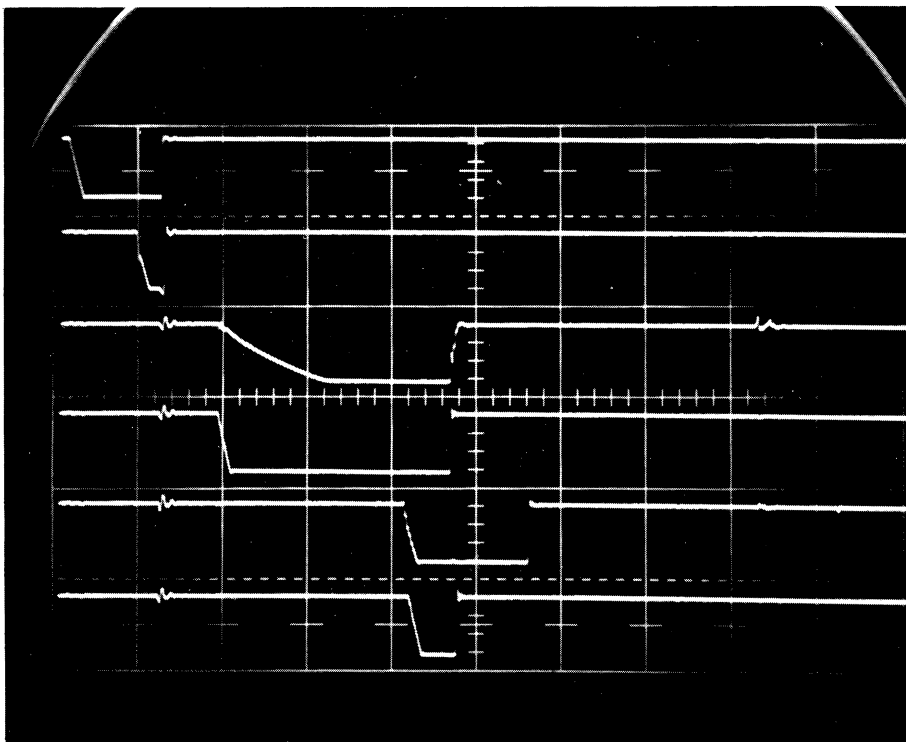
OUR ADR

BO→ARI

ADR IN(DLY)

ARI→BI

CMD OUT

BO→BRI

1.0 S CM

Fig. B6 GATE TRANSFERS

FIGURE B5

CHANNEL SEIZURE (0.5μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	ADR OUT	ADO+	1B18P	DEC +
2	OUR ADR	OURAD+	3B1ØP	DEC +
3	SEL OUT	SEO+	1A22N	DEC +
4	CU SEL	SEL+	3B1ØF	DEC +
5	CMD CYC	CMDCY+	3B12L	DEC +
6	OPL IN		1BØ1D	IBM

FIGURE B6

BUS TRANSFERS (1.0μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	OUR ADR	OURAD+	3B1ØD	DEC +
2	BO→AR1	BOAR1+	3B13P	DEC +
3	ADR IN	BADI+	3AØ9D	DEC +
4	AR1→BI	AR1BI+	3A13D	DEC +
5	CMD OUT	CMO+	1A25U	DEC +
6	BO→BR1	BOBR1+	3A13J	DEC
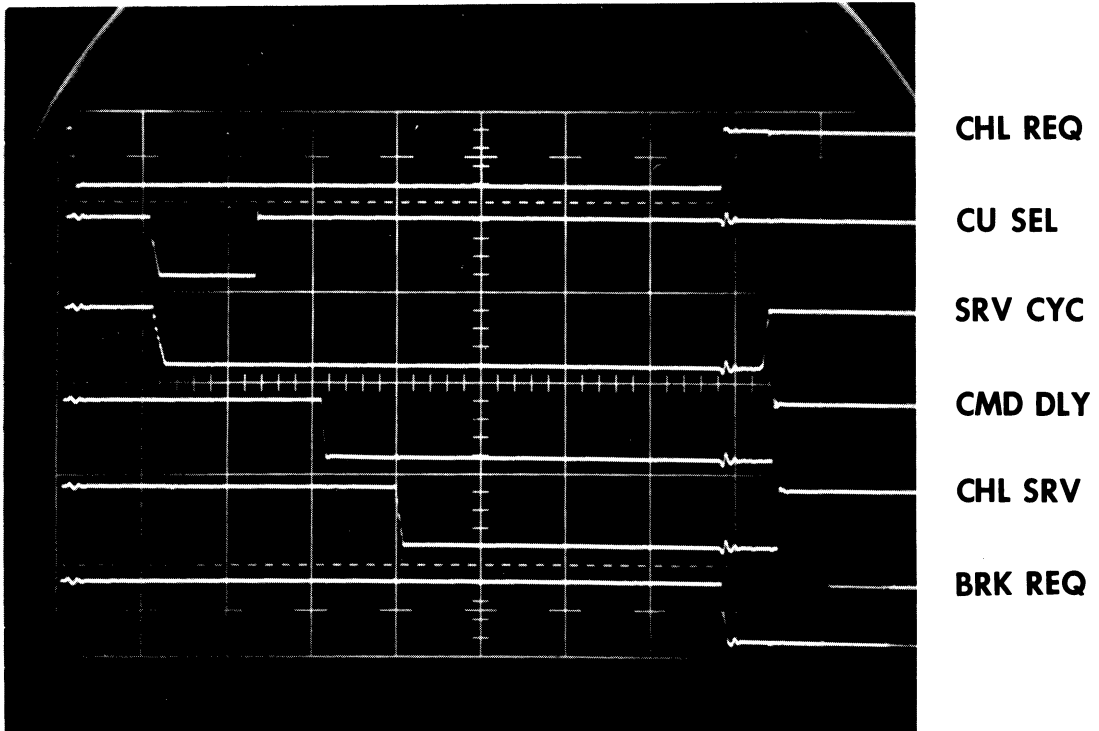
1.0μS/CM

Fig. B7   MAJOR STATE-SERVICE CYCLE
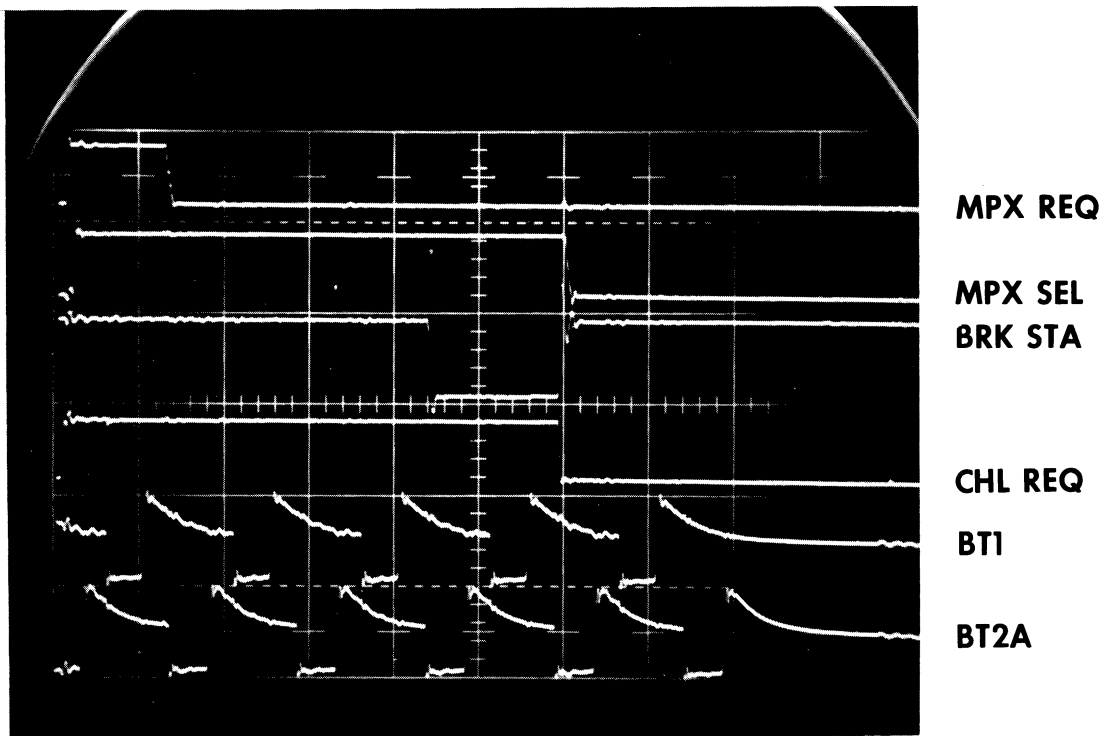
1.0μS/CM

Fig. B8   DATA BREAK-SERVICE CYCLE

FIGURE B7

MAJOR STATES-SERVICE CYCLE (1μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	CHL REQ	CHNRQ+	3B18P	DEC+
2	CU SEL	SEL+	3B1ØF	DEC+
3	SRV CYC	SRVCY+	3B13N	DEC+
4	CMD DLY	CMDLY+	3AØ7J	DEC+
5	CHL SRV	CHSRV+	3AØ7P	DEC+
6	BRK REQ	BRKRQ+	3B17P	DEC+

FIGURE B8

DATA BREAK-SERVICE CYCLE (1μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	MPX REQ	REQ1	3A17D	DEC-
2	MPX SEL	SEL1-	2B30E	DEC-
3	BRK STA	BRKSTA	1B03P	DEC+
4	CHLREQ	CHNRQ+	3B18P	DEC+
5	BT1	BT1	3B29S	DEC(P)
6	BT2	BT2A	3B29T	DEC(P)

2μS/CM

Fig. B9 TEST I/O LOOP

ADR OUT

OPL IN

CMD OUT

STA IN

SRV OUT

SUP OUT

1μS/CM
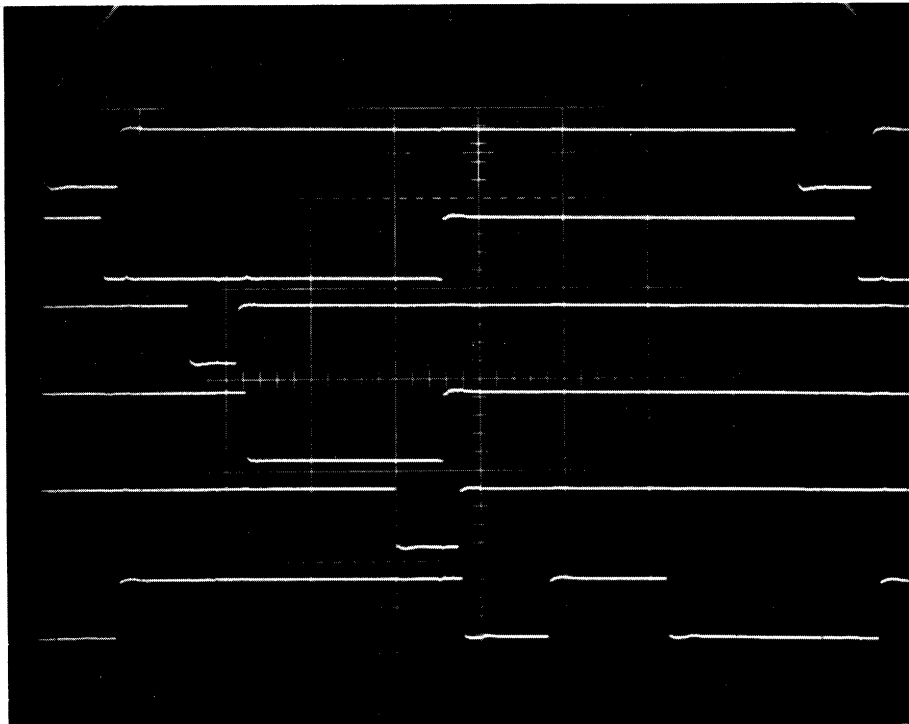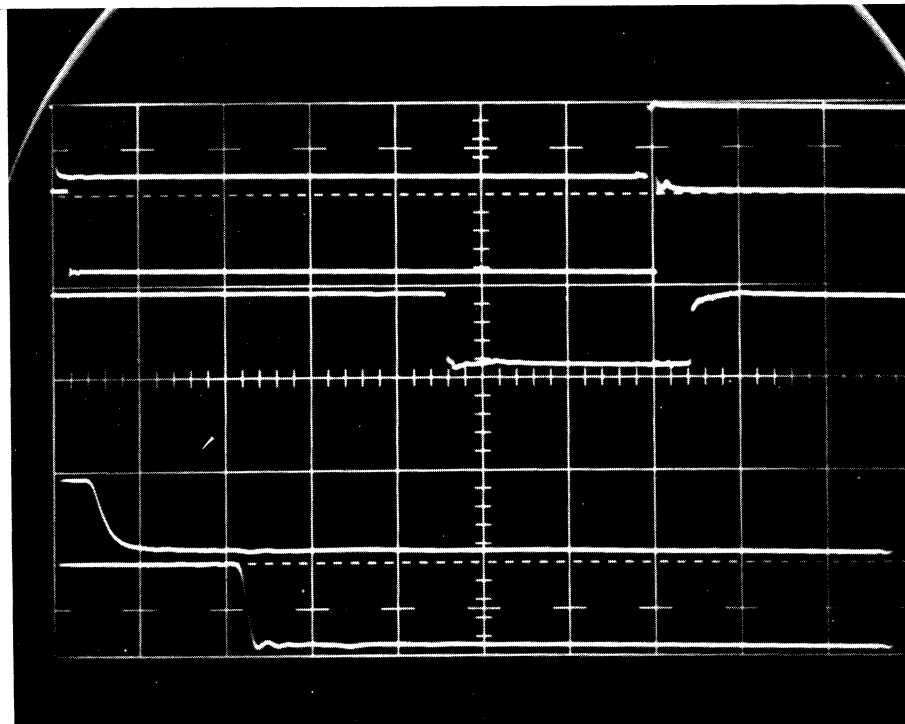
SEL OUT

SEL OUT PROP

SEL IN

0.1μS/CM

SEL OUT

SEL OUT PROP

Fig. B10 SEL OUT/SEL IN DELAYS

FIGURE B9

TEXT I/O LOOP (2μs/cm)

Line	Name	Signal Name	Pin	Polarity
1	ADR OUT	ADO	1BØ1S	IBM
2	OPL IN	OPI	1BØ1D	IBM
3	CMD OUT	CMO	1BØ1T	IBM
4	STA IN	STI	1BØ1E	IBM
5	SRV OUT	SRO	1BØ1D	IBM
6	SUP OUT	SUO	1BØ1V	IBM

FIGURE B10

SEL OUT/SEL IN DELAYS

Line	Name	Signal Name	Pin	Polarity
	(1μs/cm)			
1	SEL OUT	SEL OUT	1BØ1P	IBM
2	SEL OUT PROP	SEL PRP	1BØ2P	IBM
3	SEL IN	SEI	1BØ1M	IBM
	(0.1μs/cm)			
1	SEL OUT	SEL OUT	1BØ1P	IBM
2	SEL OUT PROP	SEL PRP	1BØ1P	IBM

APPENDIX C

ANALYSIS OF SELECT LATCH CIRCUITRY

ANALYSIS OF SELECT LATCH CIRCUITRY

The select latch consists of two interlocking flip-flops interconnected as shown in Figure C1. The outputs of one flip-flop are designated 0 and 1 in the diagram and those of the other flip-flop as 2 and 3. The latchback lines connect from 1 to 1' and 3 to 3' respectively. The request signal is designated —REQ and the select signal as SEL.

By straightforward analysis, the state table of Figure C1 is derived, which gives the outputs of the circuit as a function of the inputs. Four states may be recognized; and these are called Q, R, S, and T . (T does not appear for any output and is an unstable state.)

A transition diagram for this circuit is shown in Figure C2. The stable states are designated idle (no activity), select (this control unit selected), and bypass (some other control unit selected). Gates connected to the circuit detect the select and bypass states and inhibit propagation of SEL OUT in the bypass case. These states and the output decoding are so arranged that races between states cannot occur and so that no noise appears on any output during transitions.

The circuitry is implemented using standard modular components of about 35 nS propagation delay. Decisions and state transitions must be completed in times comparable to this.

Two of these circuits are used in the System/360 interface. One is connected to the CU SEL line and used in the channel seizure operation; and the other is connected to the CU BUSY line and used in the control unit busy operation.

INPUTS

OUTPUT

-REQ

1'

SEL

3'

0

1

2

3

NAND

NAND

NAND

NAND
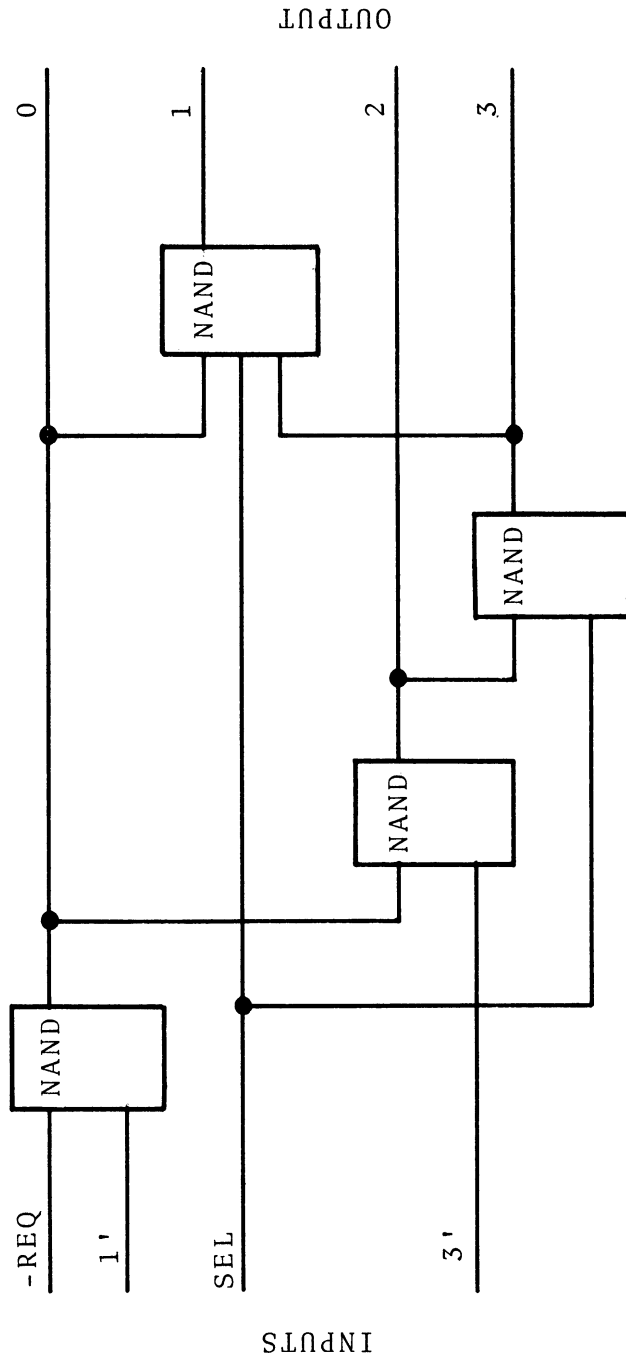
FIGURE C1. SELECT LATCH

TABLE I

INPUTS				OUTPUTS				
-REQ	SEL	1'	3'	0	1	2	3	STATE
0	0	0	0	1	1	1	1	Q
0	0	0	1	1	1	0	1	Q
0	0	1	0	1	1	1	1	Q
0	0	1	1	1	1	0	1	Q
0	1	0	0	1	1	1	0	R
0	1	0	1	1	0	0	1	S
0	1	1	0	1	1	1	0	R
0	1	1	1	1	0	0	1	S
1	0	0	0	1	1	1	1	Q
1	0	0	1	1	1	0	1	Q
1	0	1	0	0	1	1	1	Q
1	0	1	1	0	1	1	1	Q
1	1	0	0	1	1	1	0	R
1	1	0	1	1	0	0	1	S
1	1	1	0	0	1	1	0	R
1	1	1	1	0	1	1	0	R
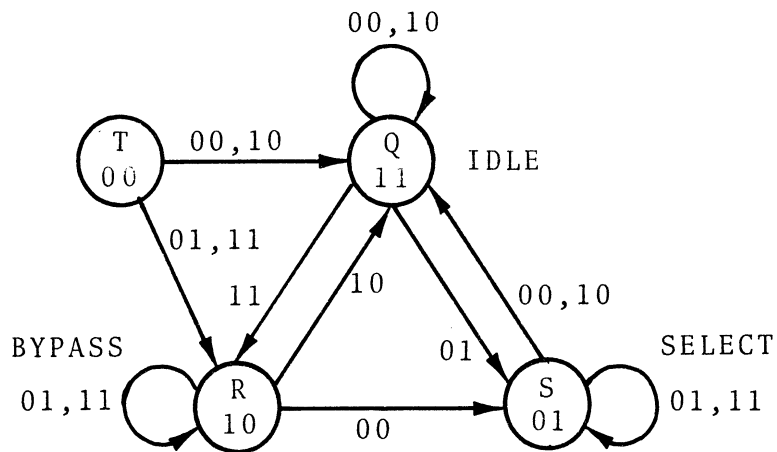
FIGURE C2. SELECT LATCH STATE TABLE

APPENDIX D

ADDITIONAL CONSTRUCTION DETAILS

ADDITIONAL CONSTRUCTION DETAILS

D1. System Configuration

The System/360 Interface as a component of the Data
Concentrator is assembled in two equipment racks which also
house a high-speed paper tape reader/punch and the various
power supplies and connectors which service the system. The
euqipment layout in these racks is shown in Figure D1. The
PDP-8 occupies one of these racks in which space is available
for further expansion of extended memory, from the now
present 12K. The other rack contains interface circuitry, the
reader/punch, and the power supplies. The top three bays con-
tain the interface circuitry itself. These bays are connected
to the Test Panel immediately below, to the PDP-8, and to the
Channel Interface connectors (bottom bay) with DEC module con-
nectors. The tape transport for both the reader and the punch
are mounted on slides immediately above the operating table
as shown. The two logic bays which service this equipment
are installed immediately below the table. Except for the
attached PDP-8 cables, which are routed through the interface,
this equipment is entirely independent of the interface.

At the bottom of the rack is a panel which carries
the four channel interface connectors. The eight cables which
connect to the Data Concentrator side of these connectors are
routed to DEC module connectors on Bays 1 and 2 above. The four
cables which connect to the IBM side of these connectors enter
through the fan hole in the bottom of the cabinet. The fan
itself has been relocated to a panel on the rear plenum door
immediately below the power supplies.

The power supplies and AC distribution system are
mounted on the rear plenum door. A resonant-transformer—
regulated supply provides +10 volts and -15 volts to the in-
terface equipment and Test Panel. A separate supply provides
various voltages to the reader/punch equipment. Power for

RACK 1   RACK2

SPARE	SPARE
PDP-8	BAY 1
	BAY 2
	BAY 3
	INDICATOR PANEL
	PCO1 TAPE READER/PUNCH

——→ TABLE

MEMORY EXTENSION	PCO1 BAY 1
	PCO1 BAY 2
	SPARE
	CHANNEL CONNECTORS
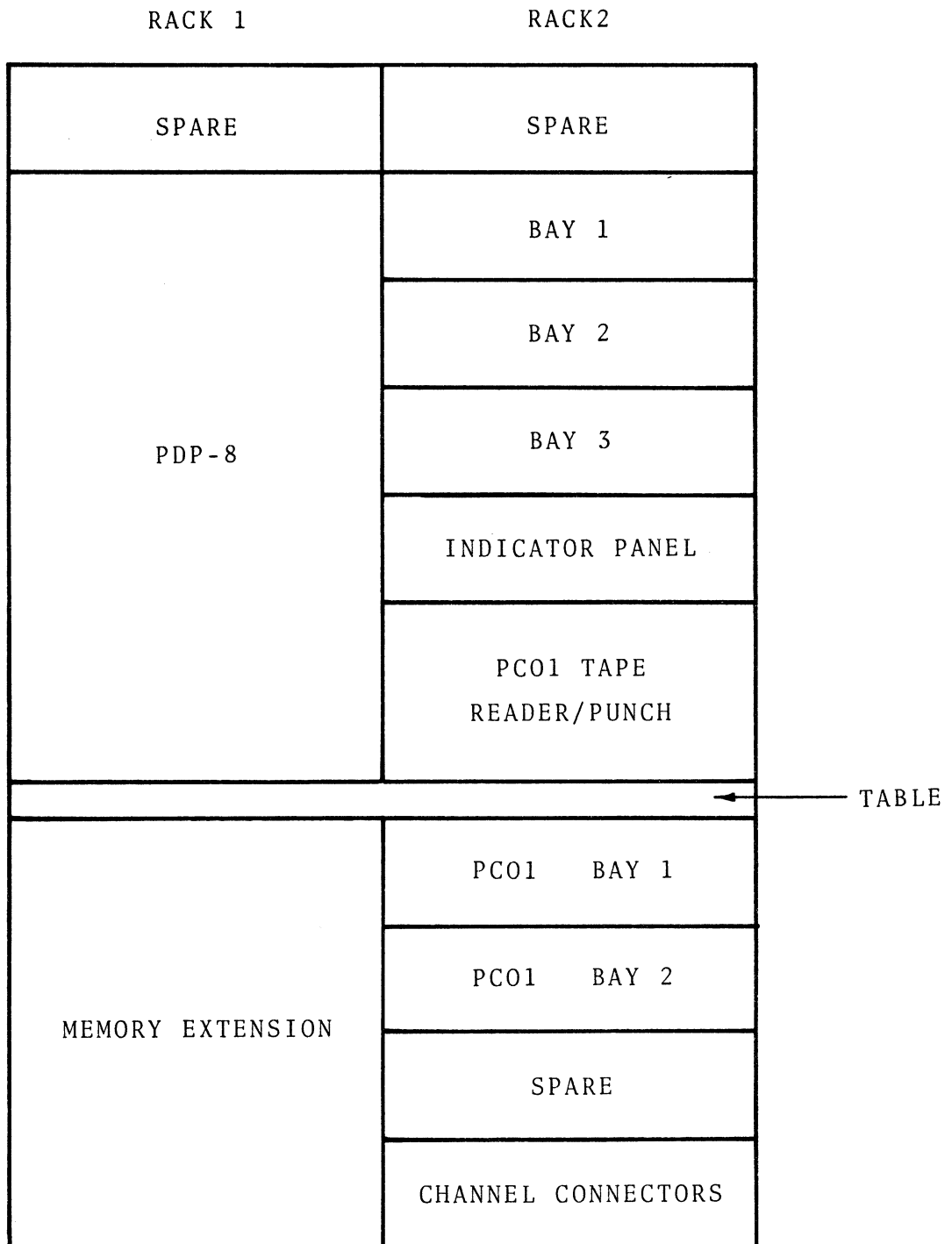
FIGURE D1.   PHYSICAL CONFIGURATION

margin-check operation is obtained from an internal supply of
the PDP-8. Switches mounted on each mounting bay allow power
for that bay to be obtained either from the regular supply
or the margin-check supply. The Power Control Unit provides
AC power to the Data Concentrator in response to control
signals issued by the parent IBM system. Power requirements
for the Data Concentrator, including the PDP-8, total about
two kilowatts at 115 VAC. A single 30-ampere circuit is used
to power the equipment.

D2. Power Control Unit

All line power to both the PDP-8 and the interface
circuitry is controlled by the Power Control Unit. This
equipment sequences power on and off in response to standardized
signals furnished by the System/360. The operation of the
equipment in response to these signals is summarized in
System/360 Power Control Interface-Original Equipment Manu-
facturers' Information, IBM Corporation, Form A22-6906-0.

The Power Control Unit (Figure D2) includes a
24V DC power supply, which is connected to the line power
at all times, and two relays. One of the relays is actuated
by the power sequence control of the channel and turns on the
line power to the PDP-8 and interface circuitry. The other
relay is actuated by a DC power supply in the interface
circuitry and enables the power sequence control of the channel
to step to the next control unit on the interface.

Two switches are used to control the operation of
the equipment. One of these, the LOCAL/REMOTE switch, is
used to transfer control of the equipment between the channel
(REMOTE) and the local controls (LOCAL) for maintenance pur-
poses. This switch should not be actuated while the equip-
ment is in the on-line state. The other switch (POWER ON/OFF)
actuates a relay which turns on line power to the PDP-8 and
interface circuitry. It is effective only when the LOCAL/
REMOTE switch is in the LOCAL state.

FIGURE D2. POWER CONTROL UNIT

D3. IBM/DEC Interface Modules

The accompanying circuits have been designed to provide IBM/DEC compatibility in a package appropriate for installation in DEC 1943 Mounting Panels. Characteristics have been chosen to satisfy the requirements outlined in System/360 I/O Interface—Channel-to-Control Unit Original Equipment Manufacturers' Information, Form A22-6843. None of the available DEC modules satisfy these requirements, notably that which specifies that the components not disturb the interface bus lines in the event of power failure or off-line operation.

BUS DRIVER (Figure D3)

Input

DEC standard levels of -3v and ground. The circuit acts as an AND for negative true-valued inputs and as an OR for positive inputs. Other input characteristics are identical to those of the R111 Diode Gate.

Output

IBM Standard SLT bus levels of ground and +3v. SLT conventions assign a logical 0 to ground level and a logical 1 to +3v. The leakage in the 0 state is less than 1nA at +3v and the output voltage in the 1 state is 3.85V at 59.3 mA and 4.5 at 30 µA. In a power-off condition the leakage in either state is less than 1nA.

Performance

Propagation delay is 45ns for output rise (0 to +3V) and 25ns for output fall (+3v to 0). Transition time is 20ns for output rise and 10ns for output fall. Characteristics are not significantly affected for power supply variation of ±5V on either the +10V or the -15V supply.
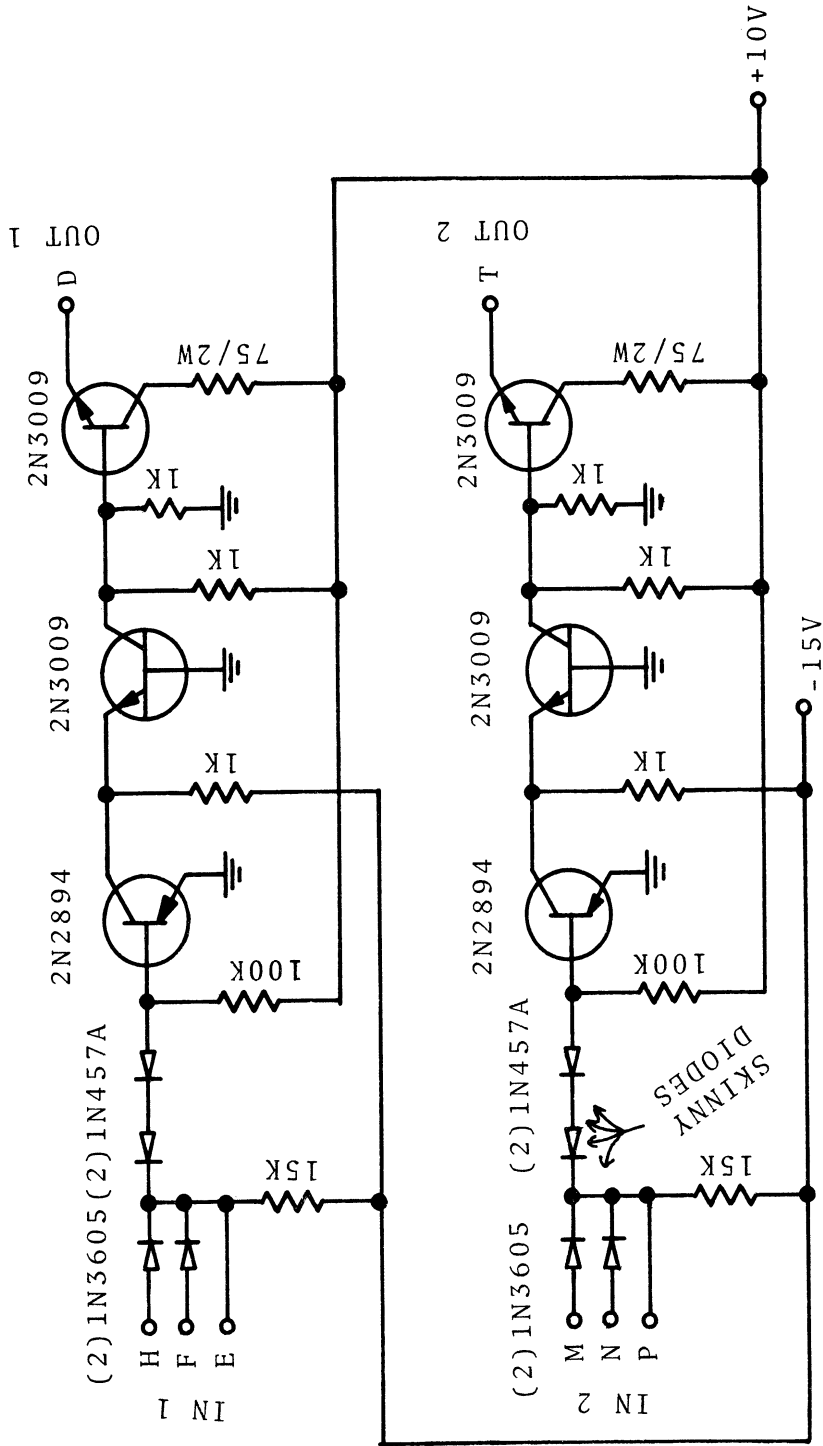
FIGURE D3. DEC TO IBM BUS DRIVER MODULE.

BUS RECEIVER (Figure D4)

Input

IBM standard SLT bus levels of ground and +3V. SLT
conventions assign a logical 0 to ground level and a logical
1 to +3v. The circuit is non-inverting. Input bus load-
ing is +250μA at +3V and -90μA at ground. (+equals conven-
tional current into the receiver input.) The input impedance
(at 1kc/s) is 10K ohms. In a power-off condition the input
bus is loaded at 285μA for an input voltage level of +3v,
and linearly decreases to zero as the input voltage falls
to zero.

Output

DEC standard levels of -3v and ground. Output
characteristics are identical with those of the R111 Diode
Gate.

Performance

Propagation delays and transition times are all
20ns for both output rise and output fall. Characteristics
are not significantly affected for power supply variations
of ±5V on either the +10V or -15V supply.

SELECT—OUT BYPASS (Figure D5)

This module contains an encapsulated DPDT relay,
together with its driving circuitry, and in addition an
electronic switch which provides termination for the SEL OUT
signal on the channel-control unit interface cables. The
terminator is a 92-ohm resistor. Bus voltage levels are
expected to be in the range zero to +5V.

Inputs

DEC standard levels of -3v and ground. Relay driver:
ground level activates relay armature. Terminator switch:
ground level causes terminator to be disconnected.
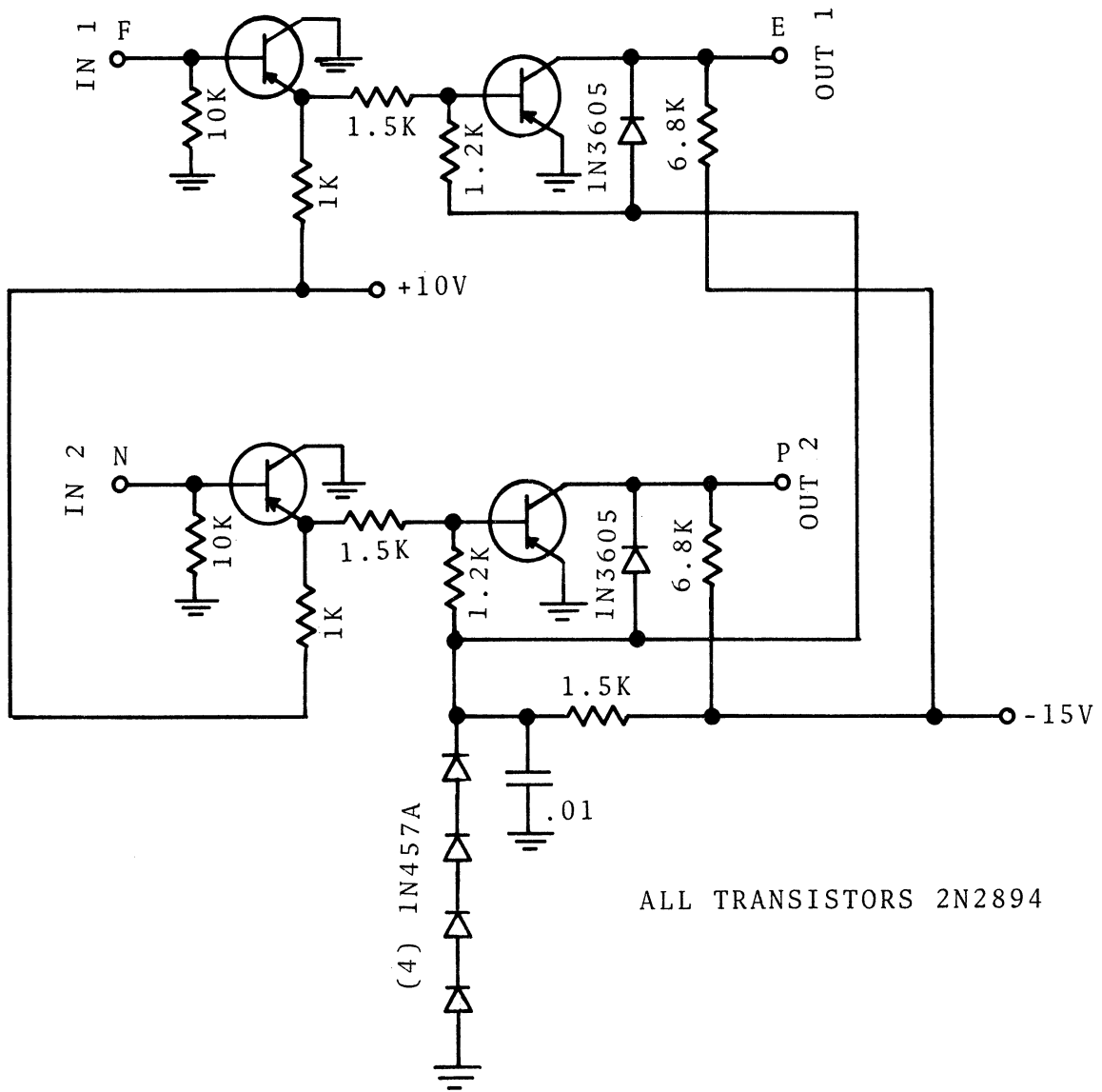
FIGURE D4.   IBM TO DEC BUS RECEIVER MODULE
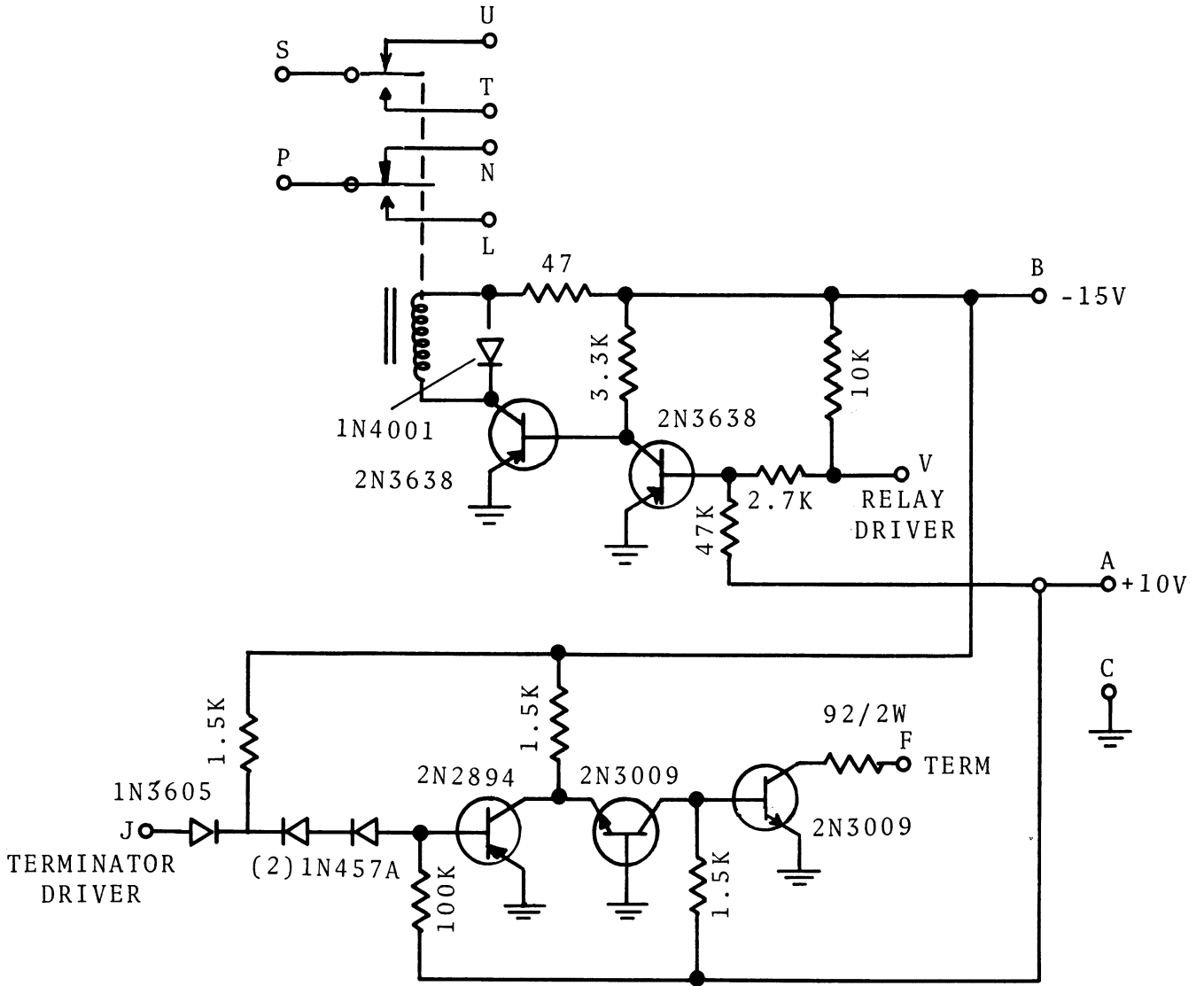
FIGURE D5.   SEL OUT BYPASS MODULE

APPENDIX E

LOGIC DIAGRAMS
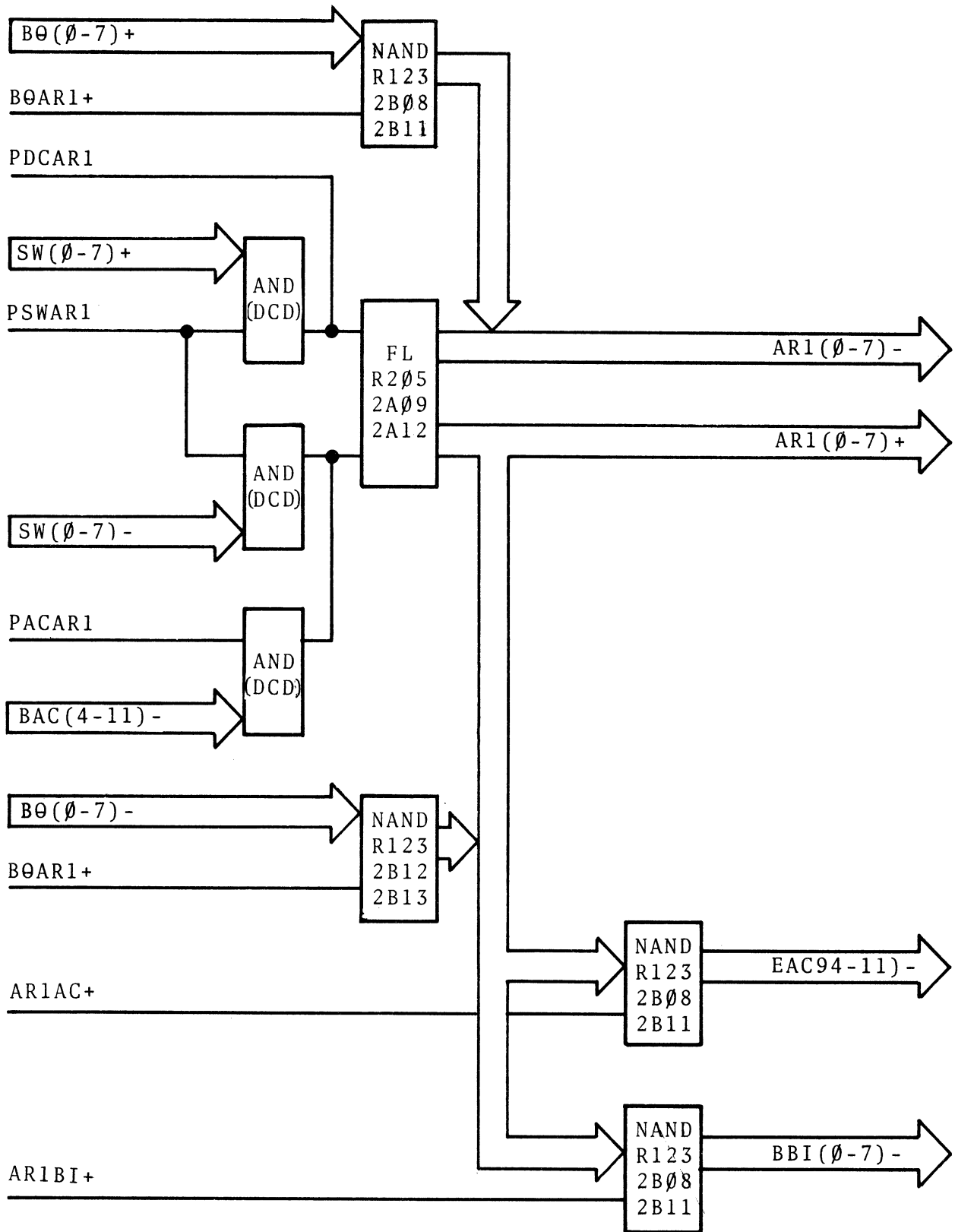
FIGURE E1. AR1
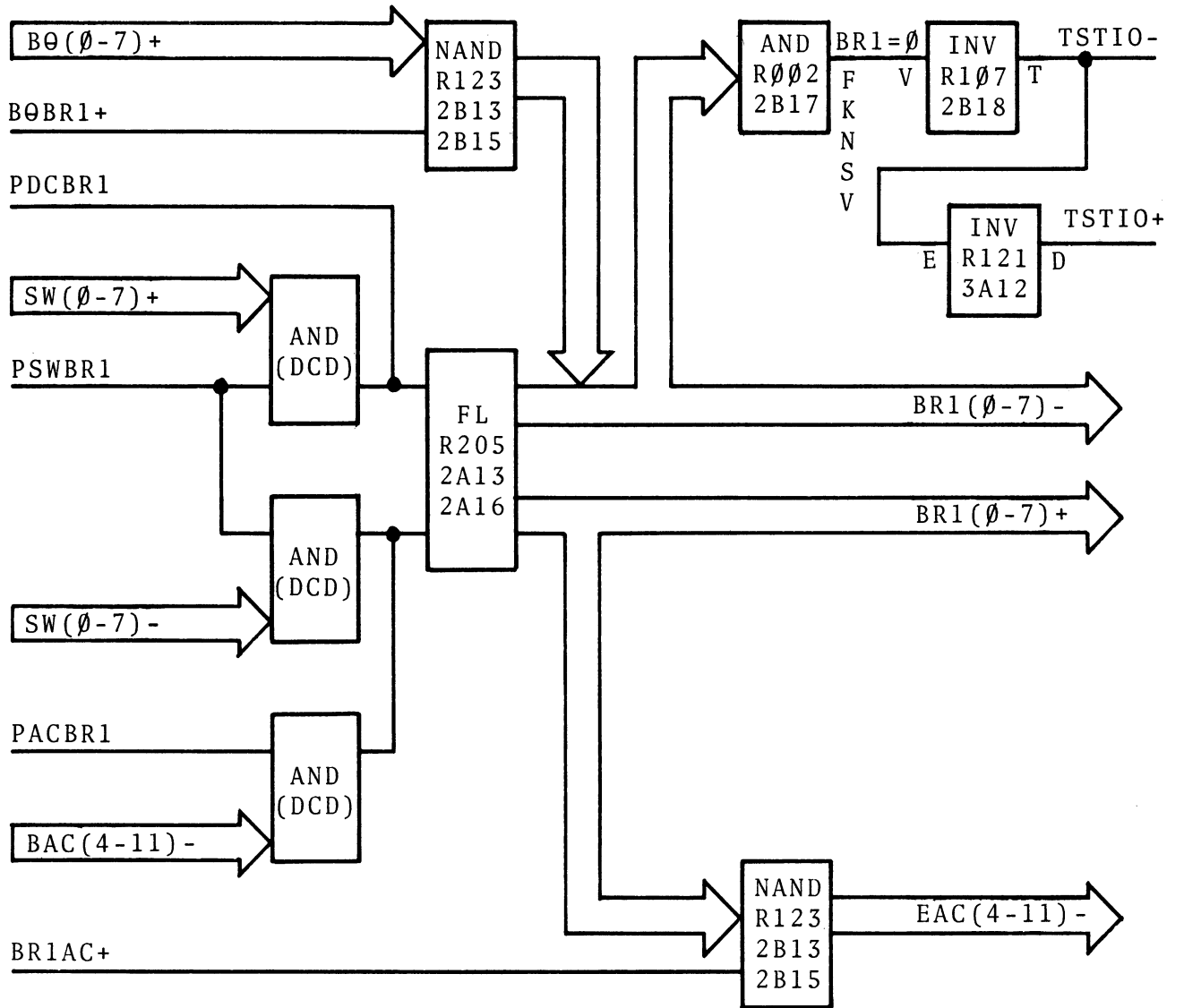
FIGURE E2.   BR1
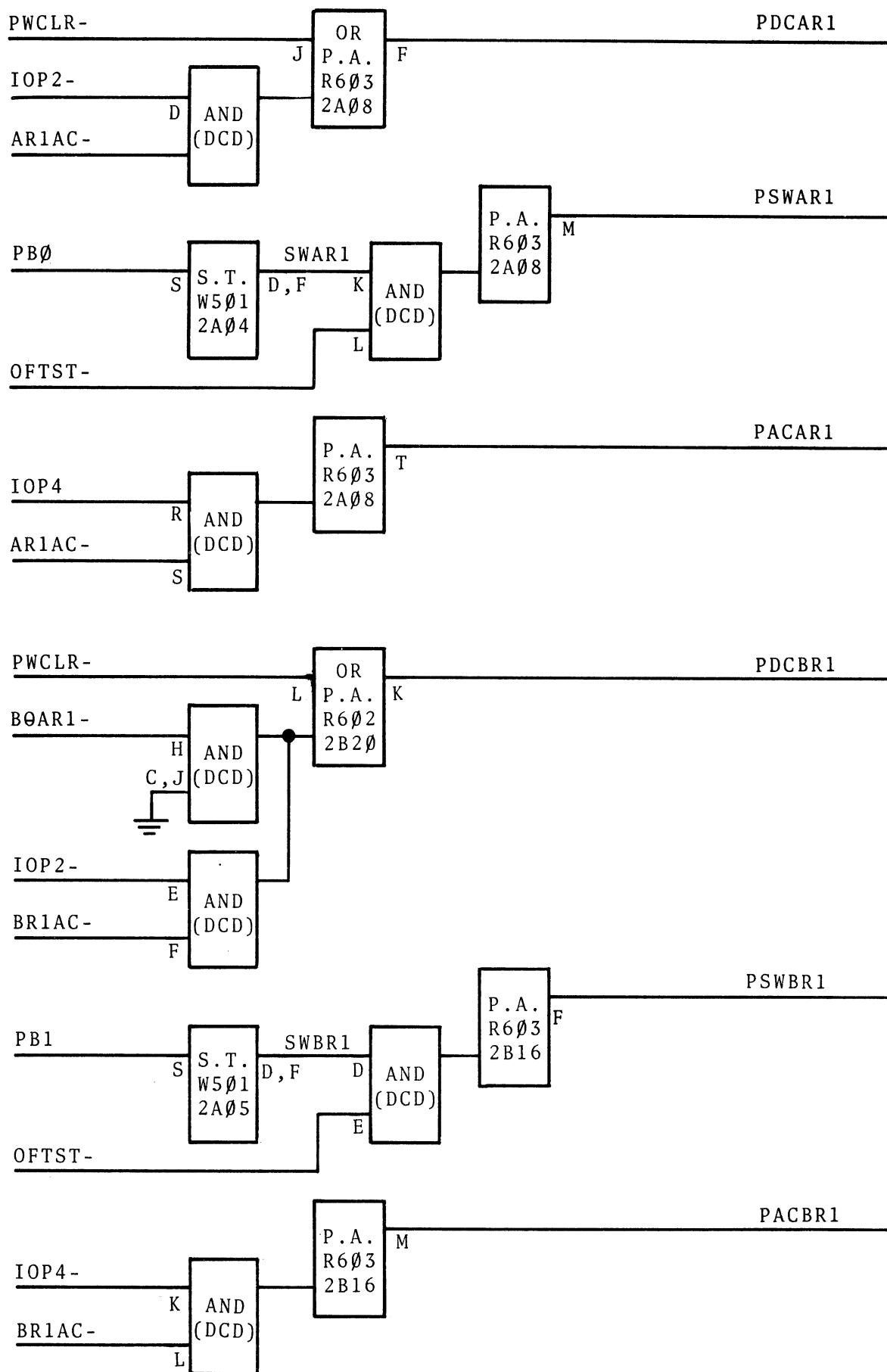
FIGURE E3.   AR1/BR1 PULSING
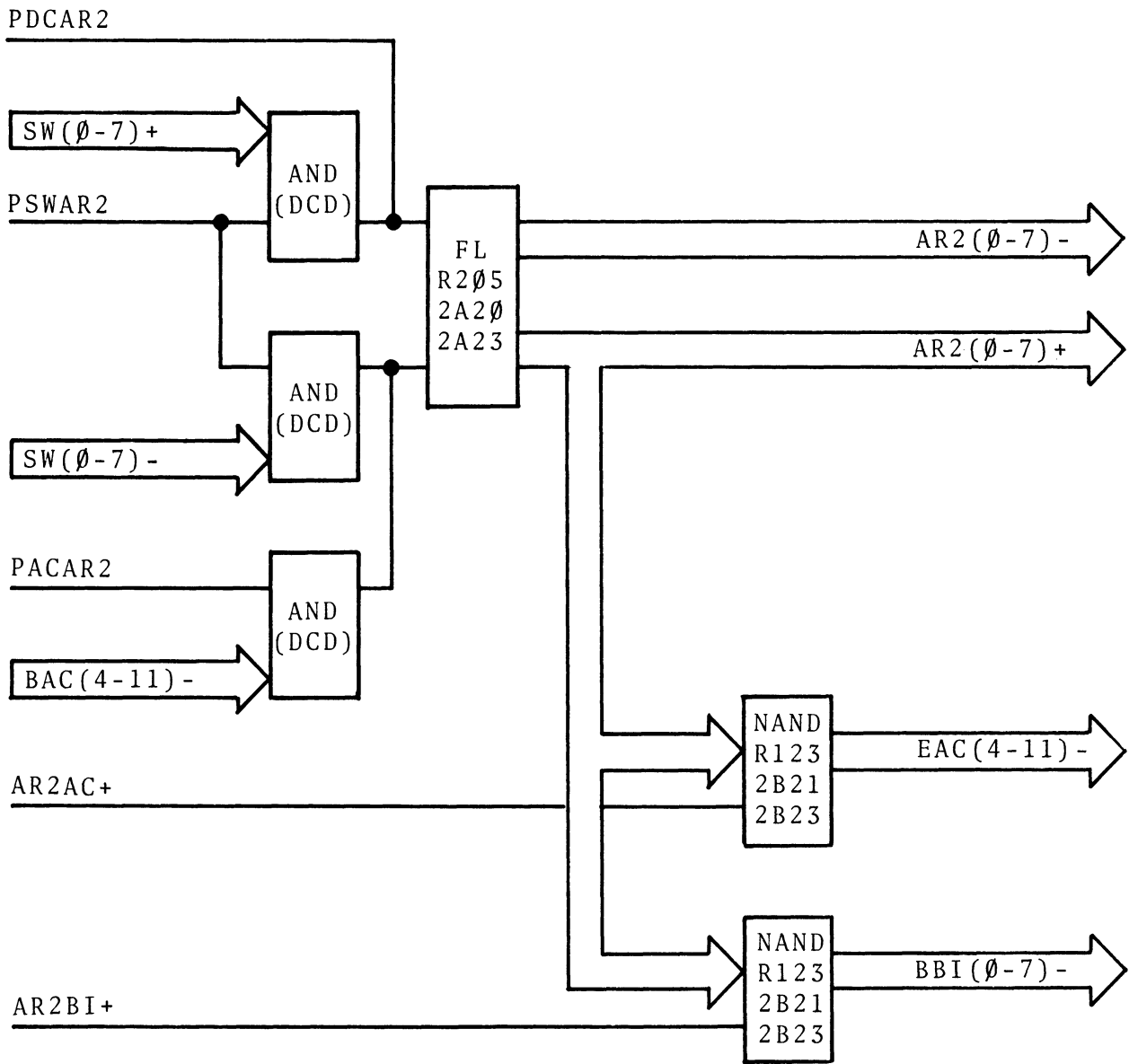
FIGURE E4. AR2
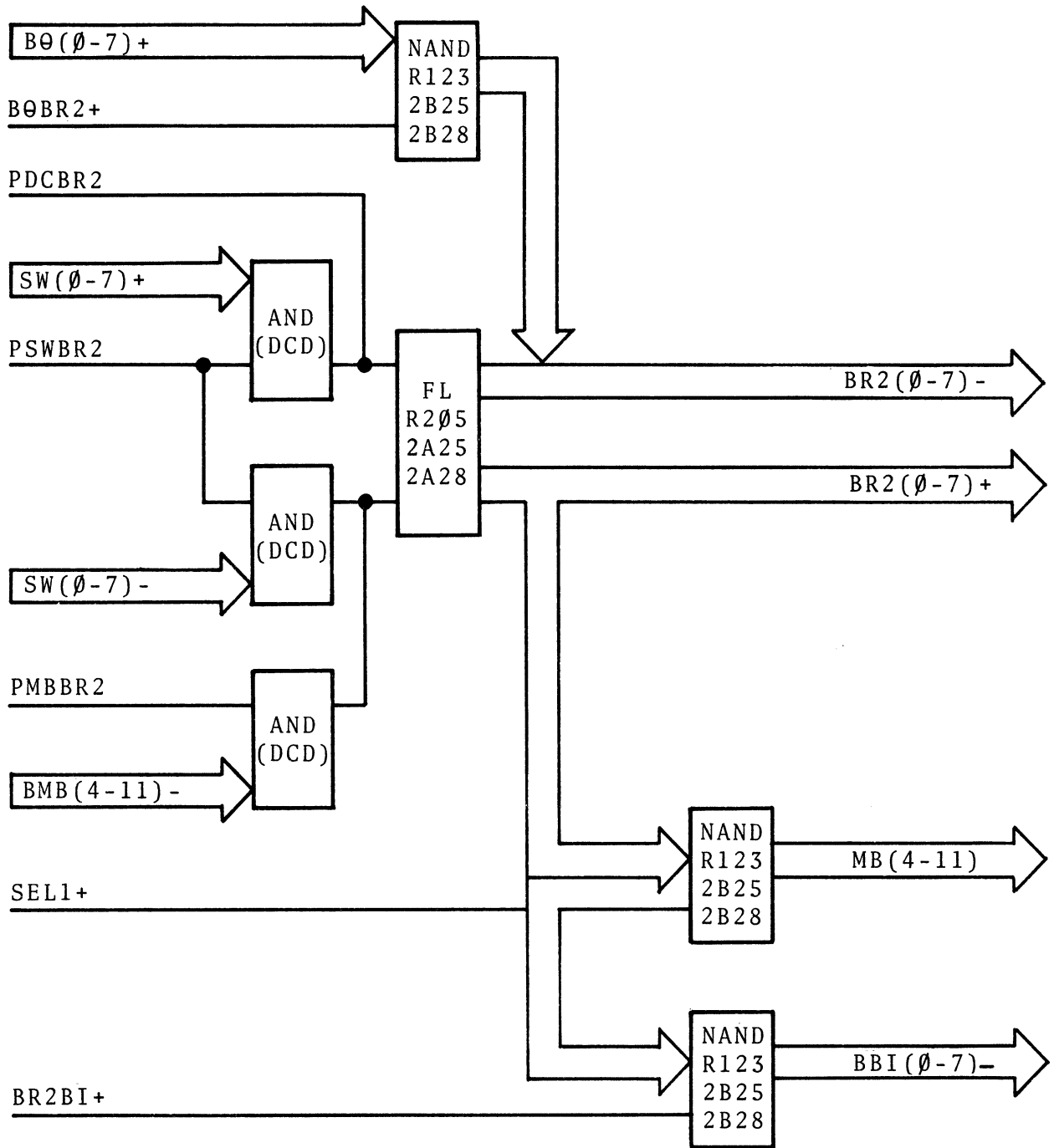
FIGURE E5. BR2
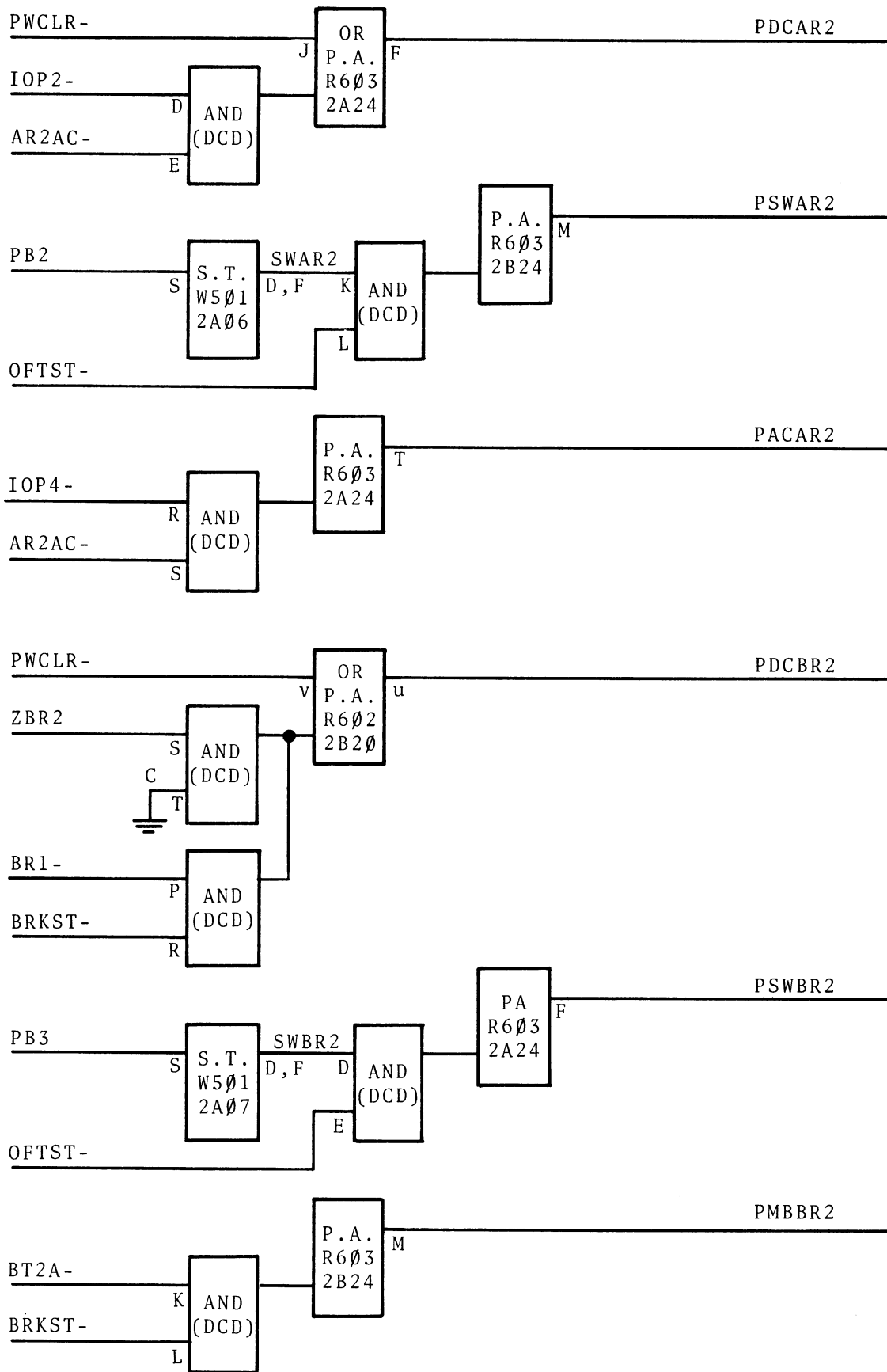
FIGURE E6. AR2/BR2 PULSING
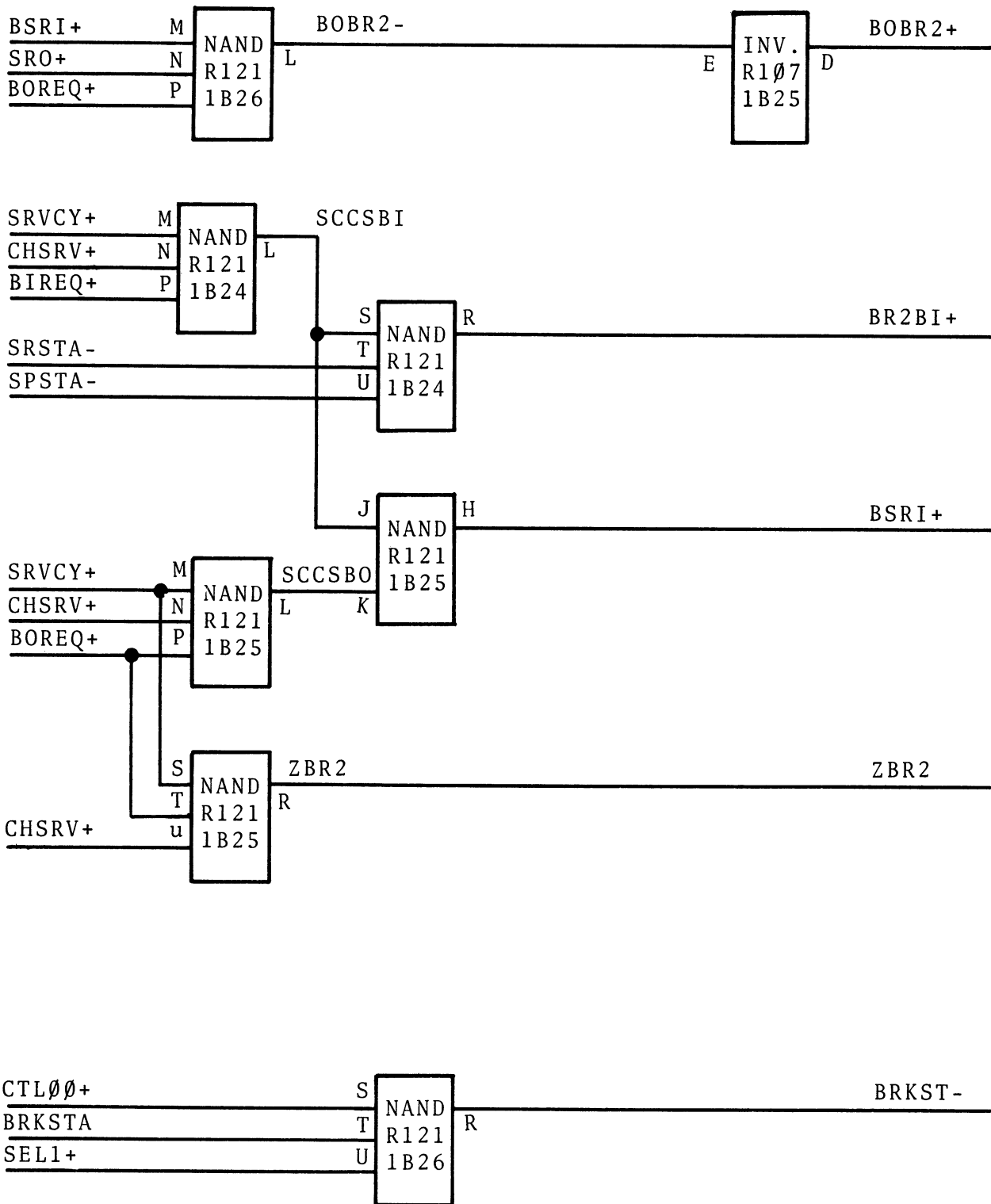
FIGURE E7. BR2 GATING

-108-
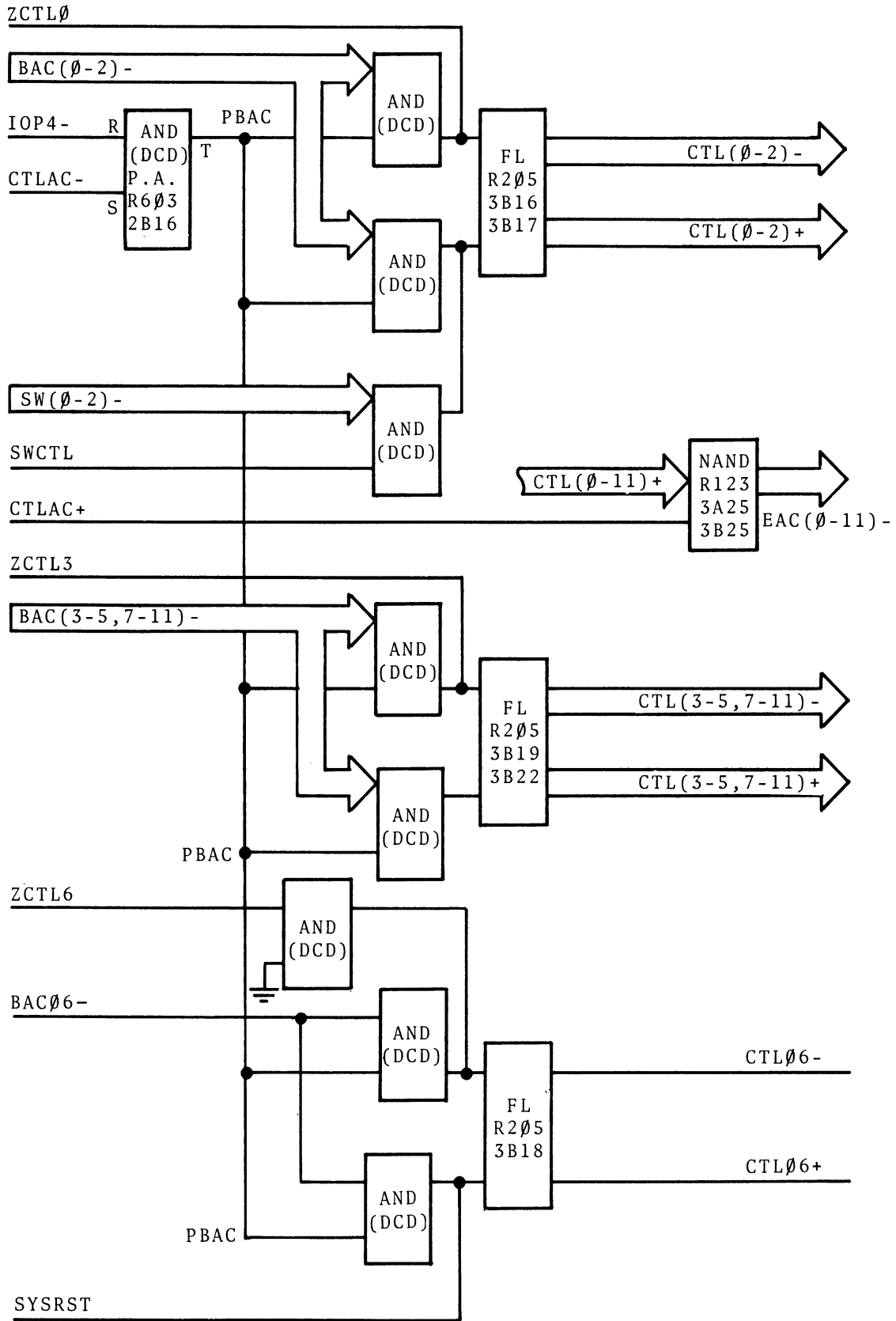
FIGURE E8. CONTROL REGISTER
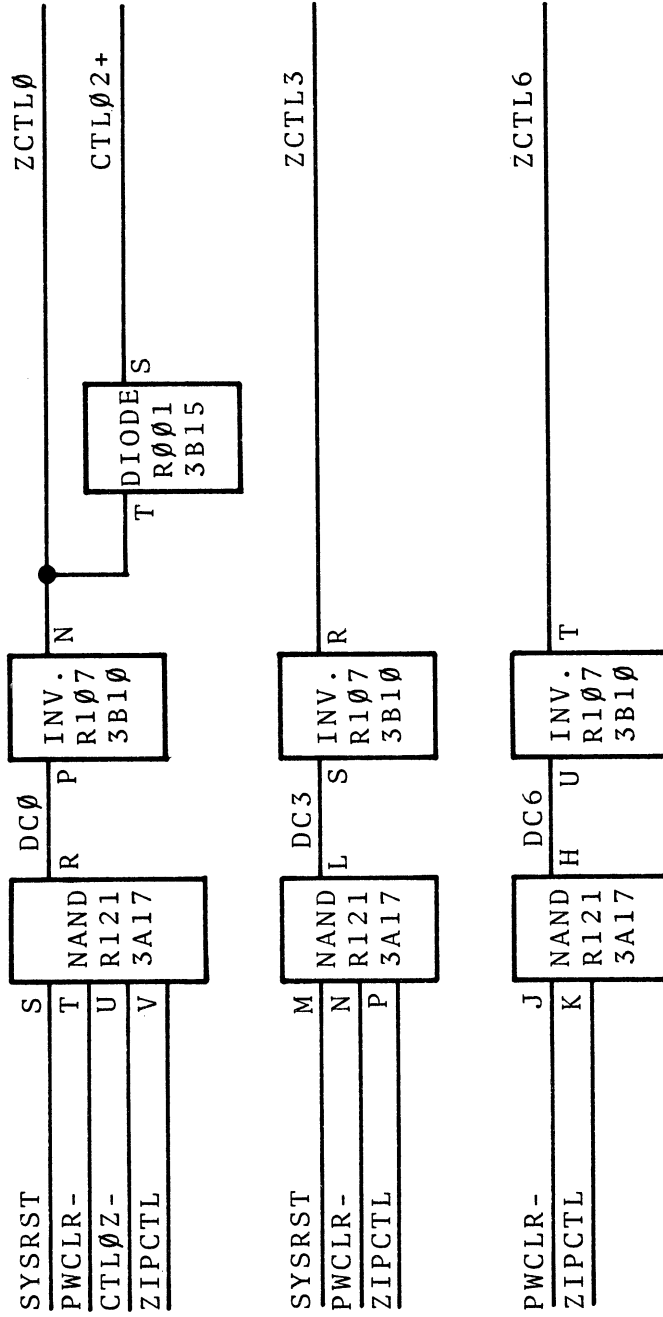
FIGURE E9. CLEARING THE CONTROL REGISTER
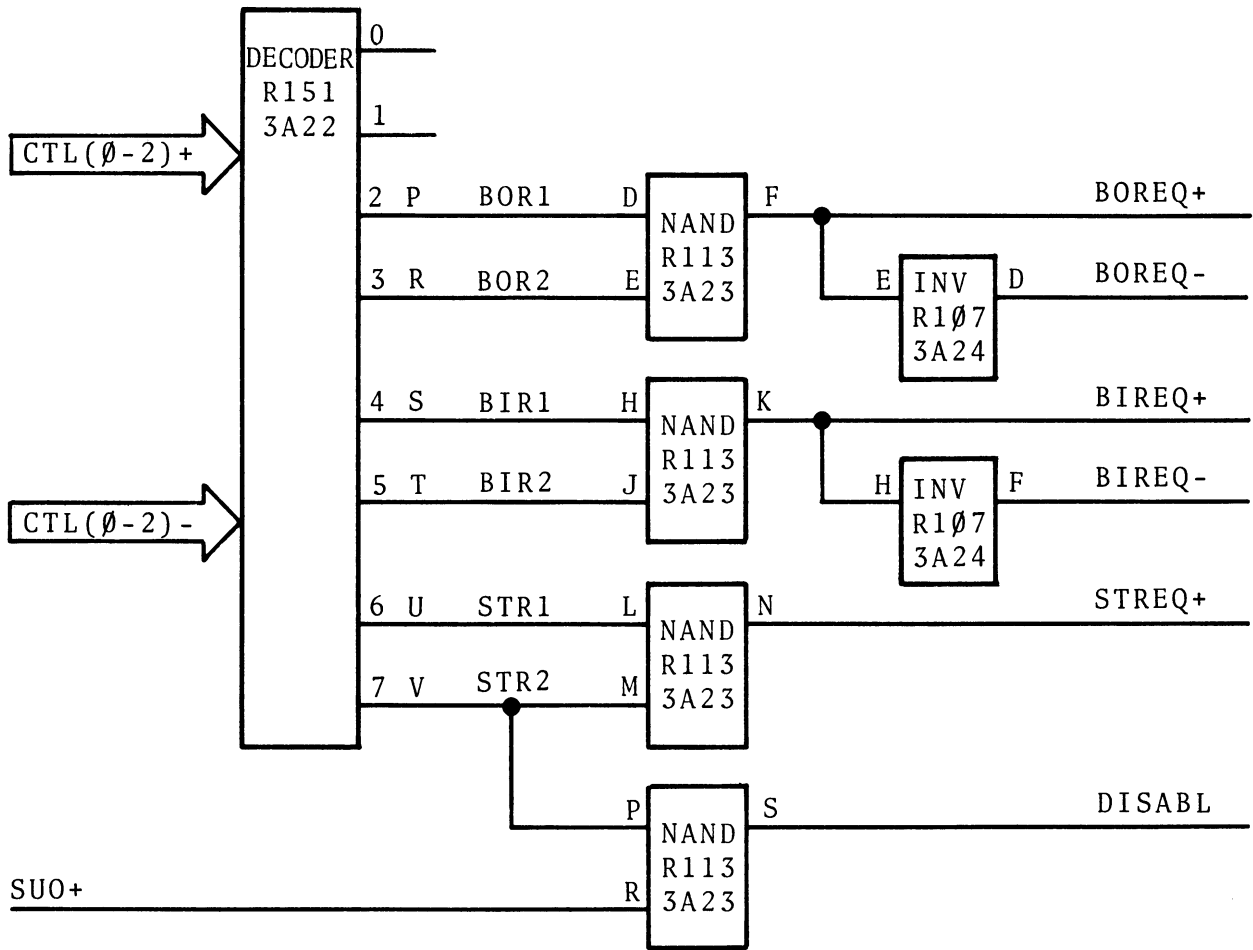
FIGURE E10:   CONTROL OPERATION DECODER
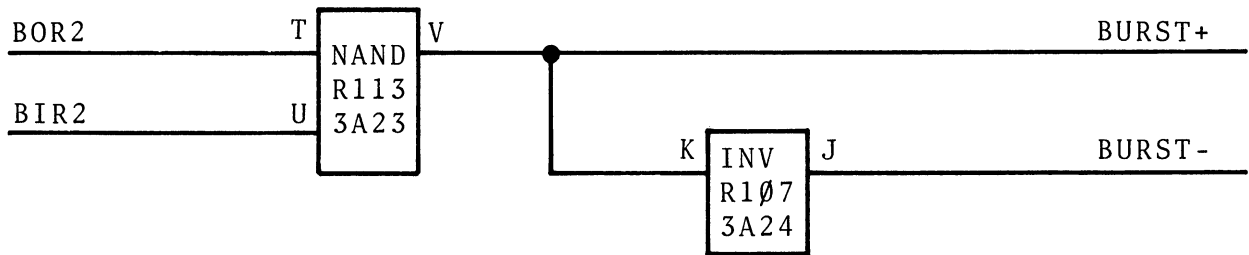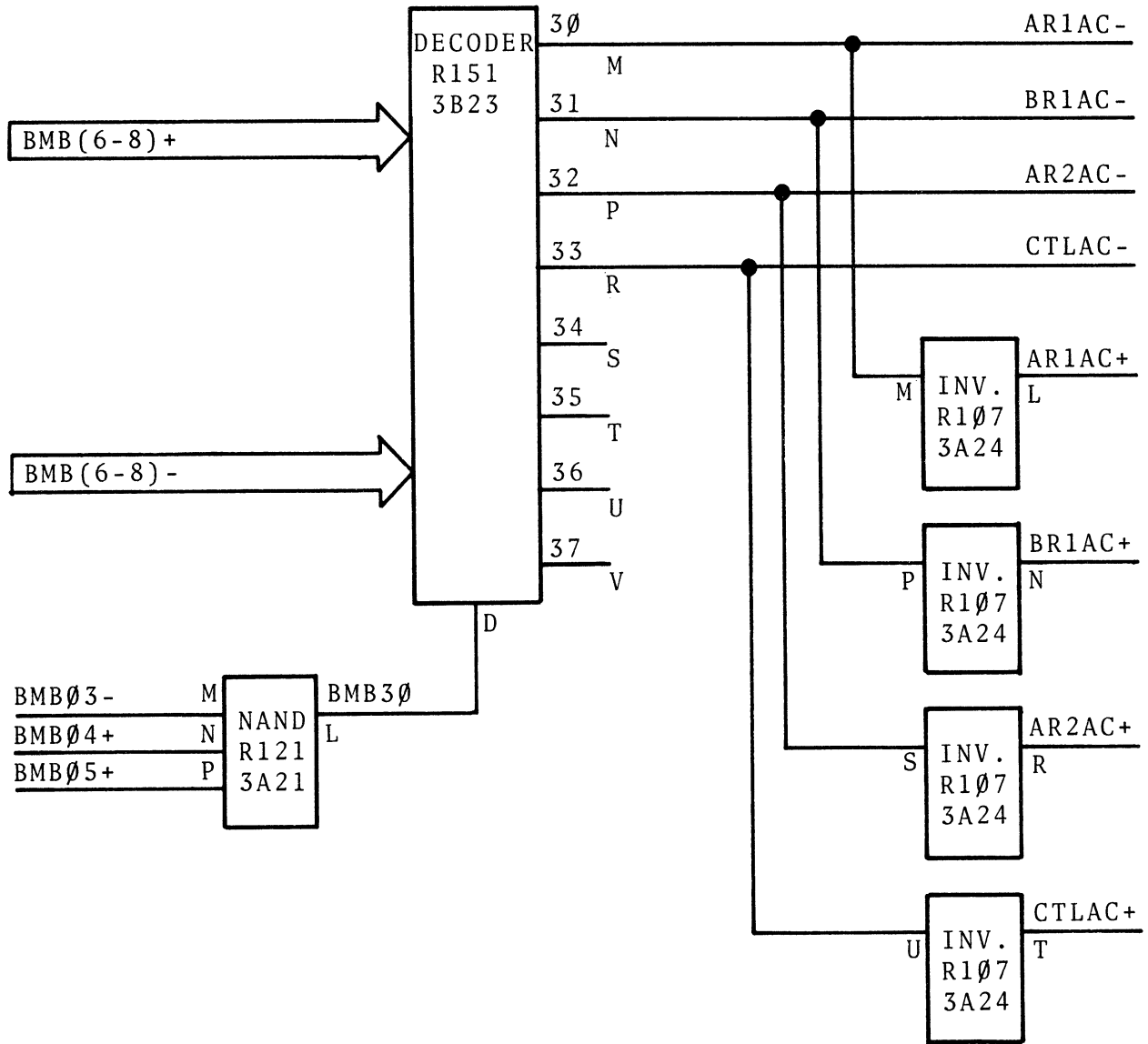
FIGURE E11: IOT DETECTION

READ ENABLE

TRANSFER DIRECTION

FIGURE E12.

3B24

D-S

EAC(∅-11)-

BAC(∅-11)-   INV.
R1∅7
3A27
3B27   BAC(∅-11)+

AND
/NOR
R141
3A26
3B26   D

3B24

T   ACTEST

MASK TEST

EAC(∅-11)+

EACAC+   NAND
R123
3A∅5
3B∅5   AC(∅-11)

GATE EAC   AC

EAC(∅-11)-   INV.
R1∅7
2B18
2B19   EAC(∅-11)+

SW(∅-7)+   INV.
R1∅7
2A29
2B19   SW(∅-7)-

AR1(∅-7)+

AR2(∅-7)-

AR1(∅-7)-

AR2(∅-7)+   AND

AND   NOR
R141
2A17
2A19   D

3B14

J   AR=AR
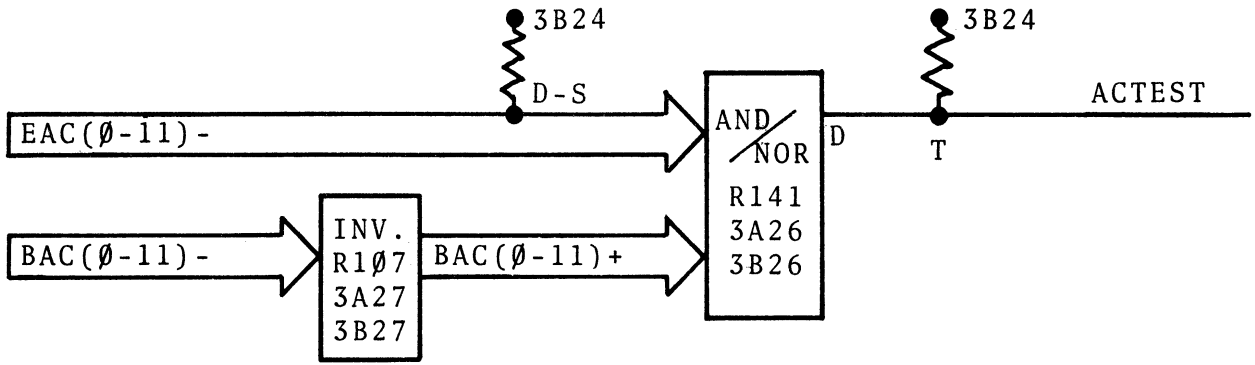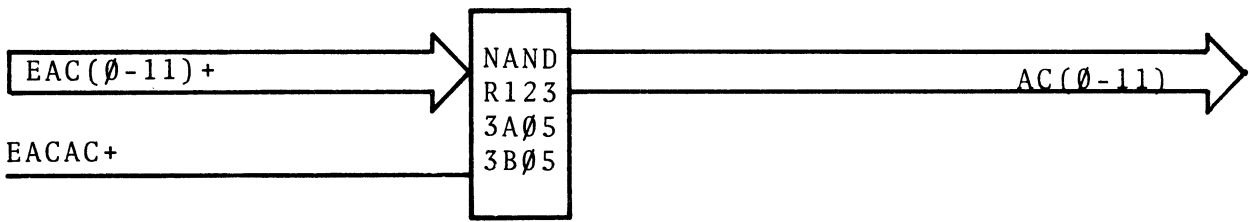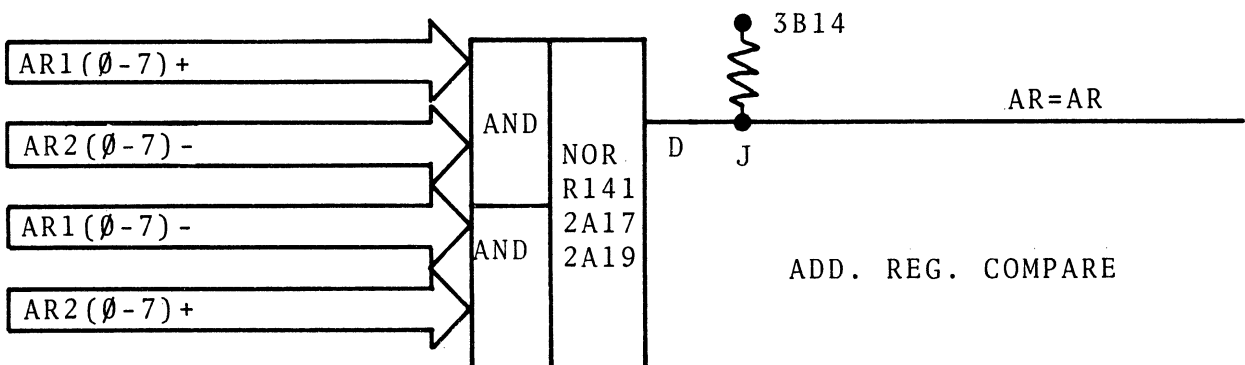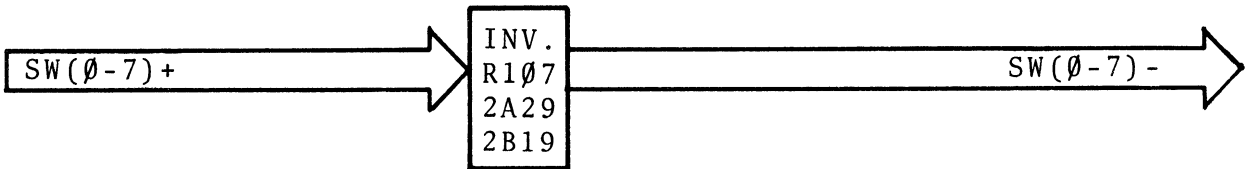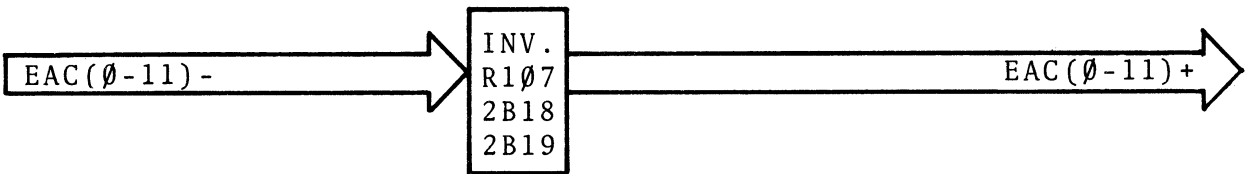
ADD. REG. COMPARE

FIGURE E 13.
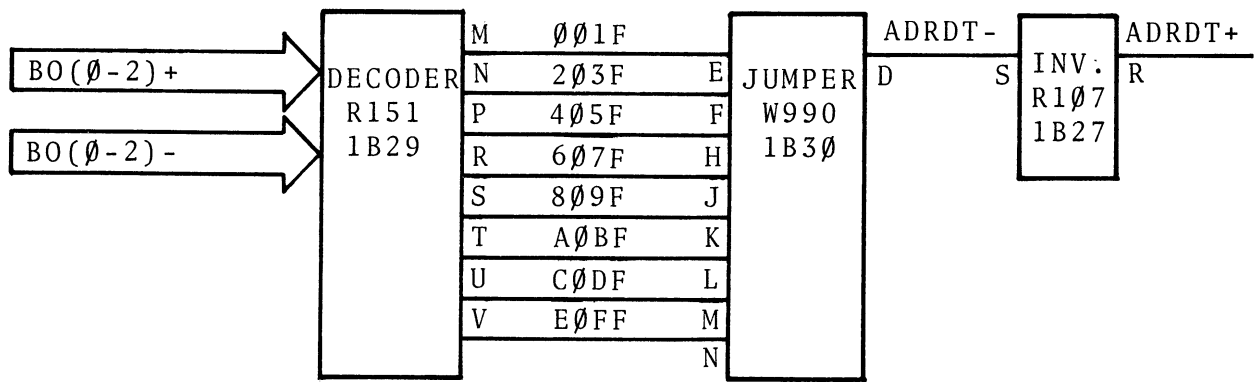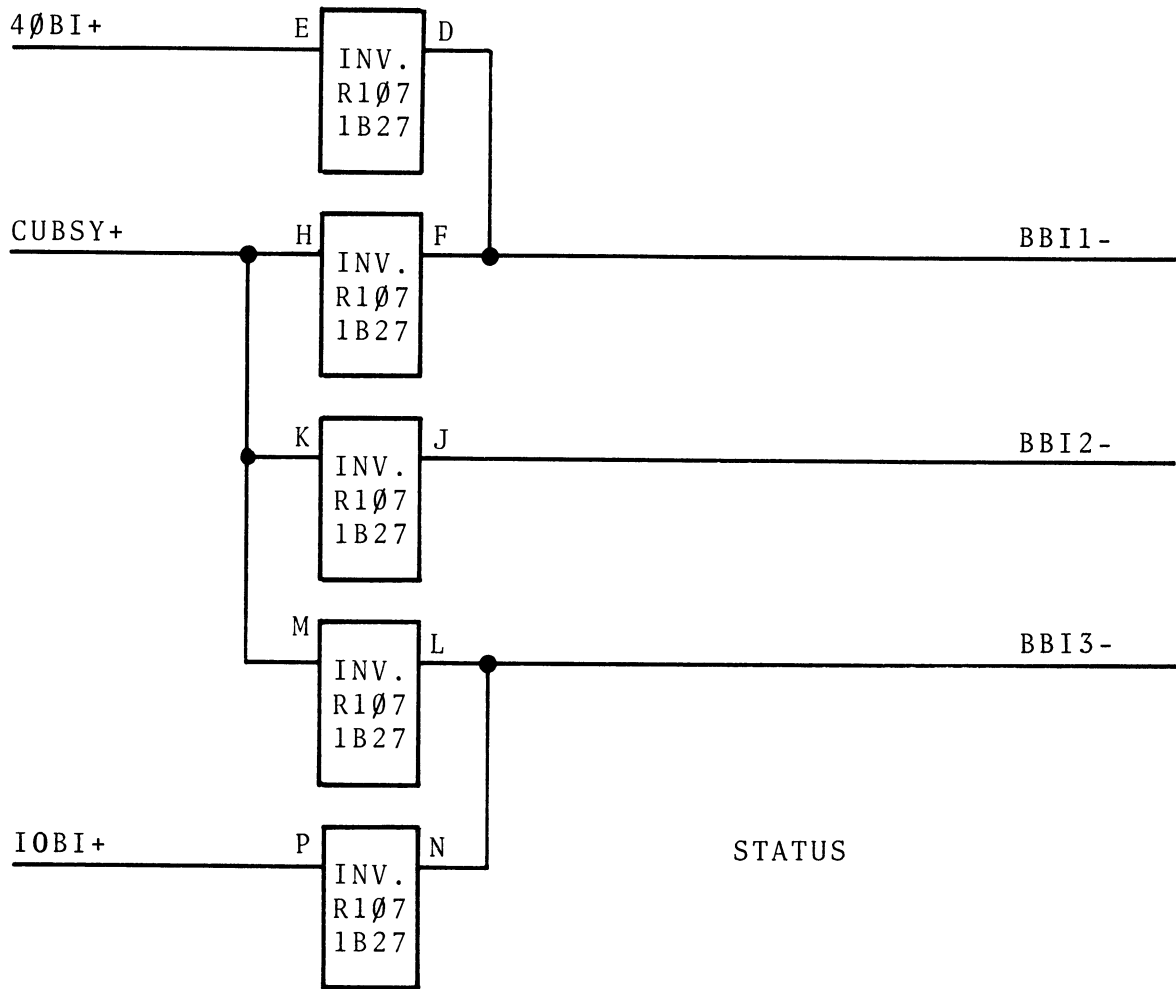
STATUS

ADDRESS DETECT

FIGURE E14.
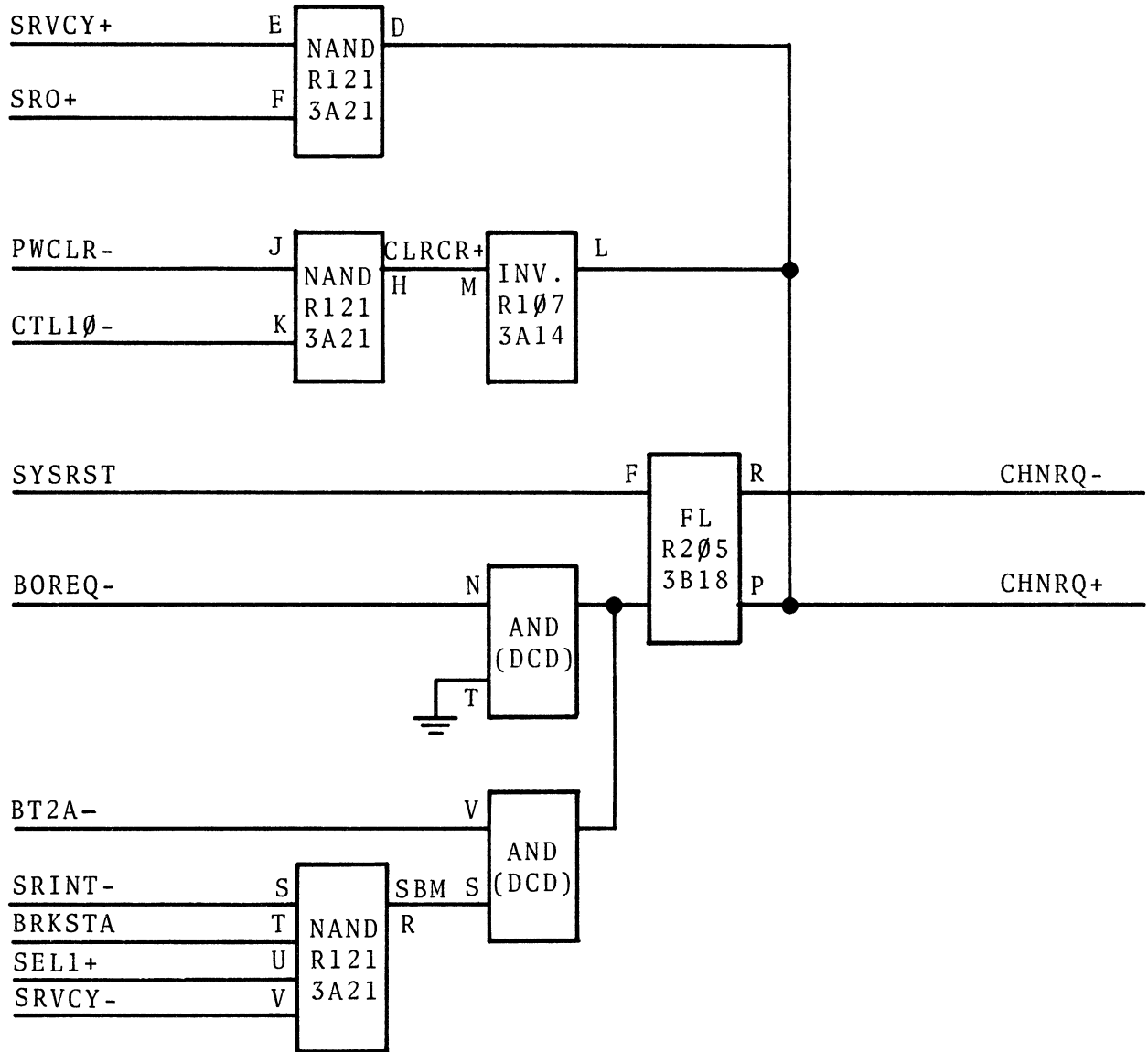
CHANNEL REQUEST

FIGURE E15.
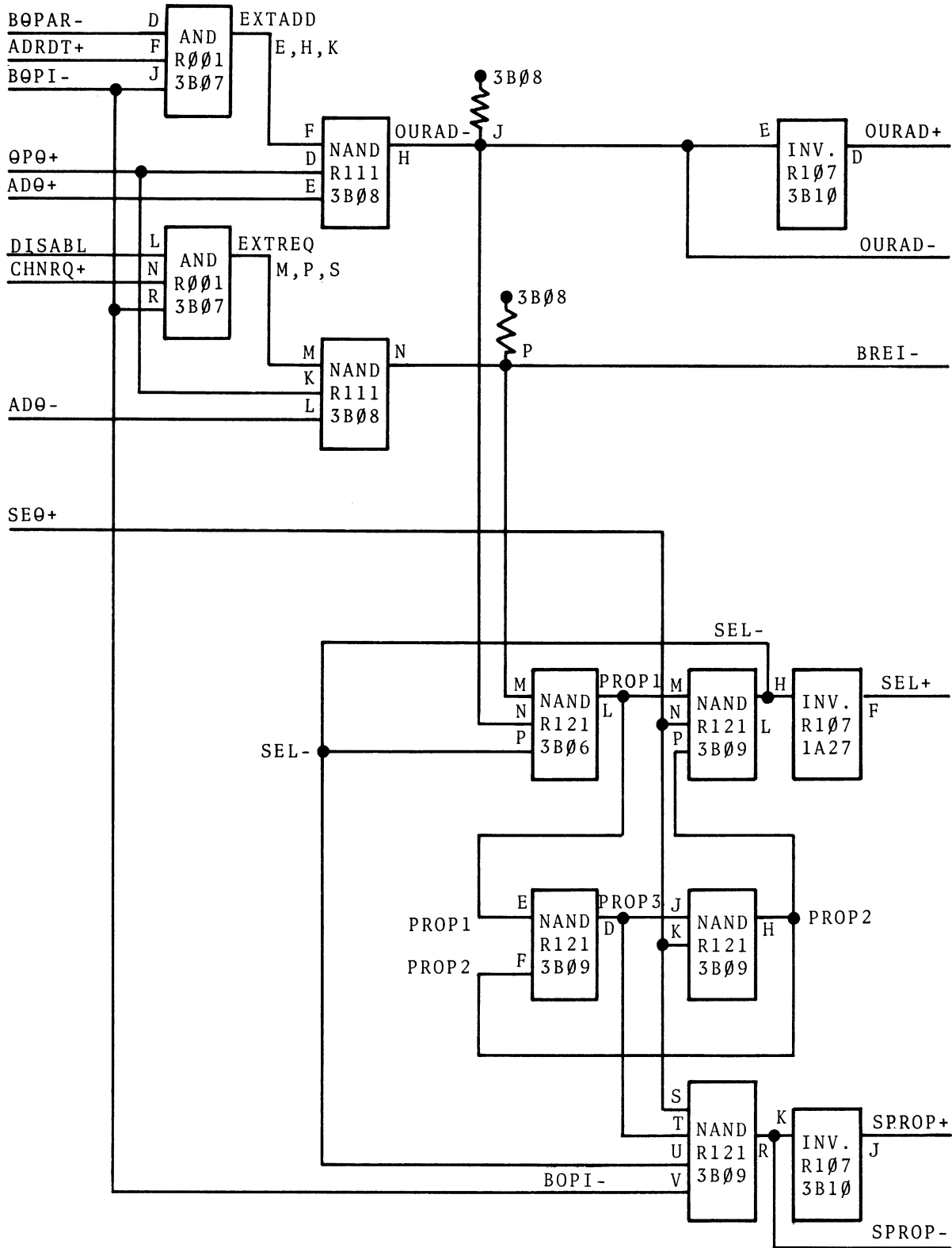
FIGURE E16.   SELECT INTERCEPTION
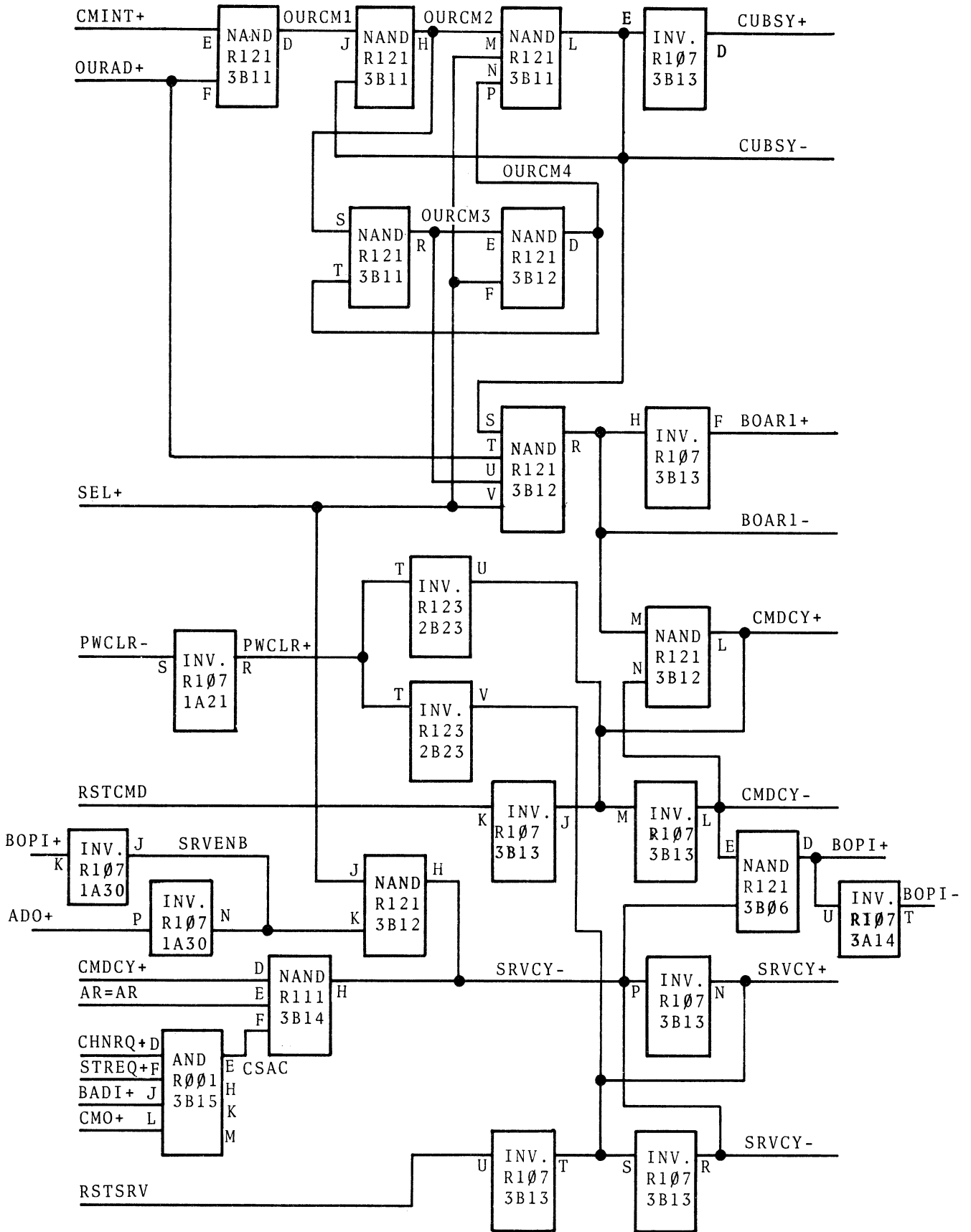
FIGURE E17. CHANNEL SEIZURE
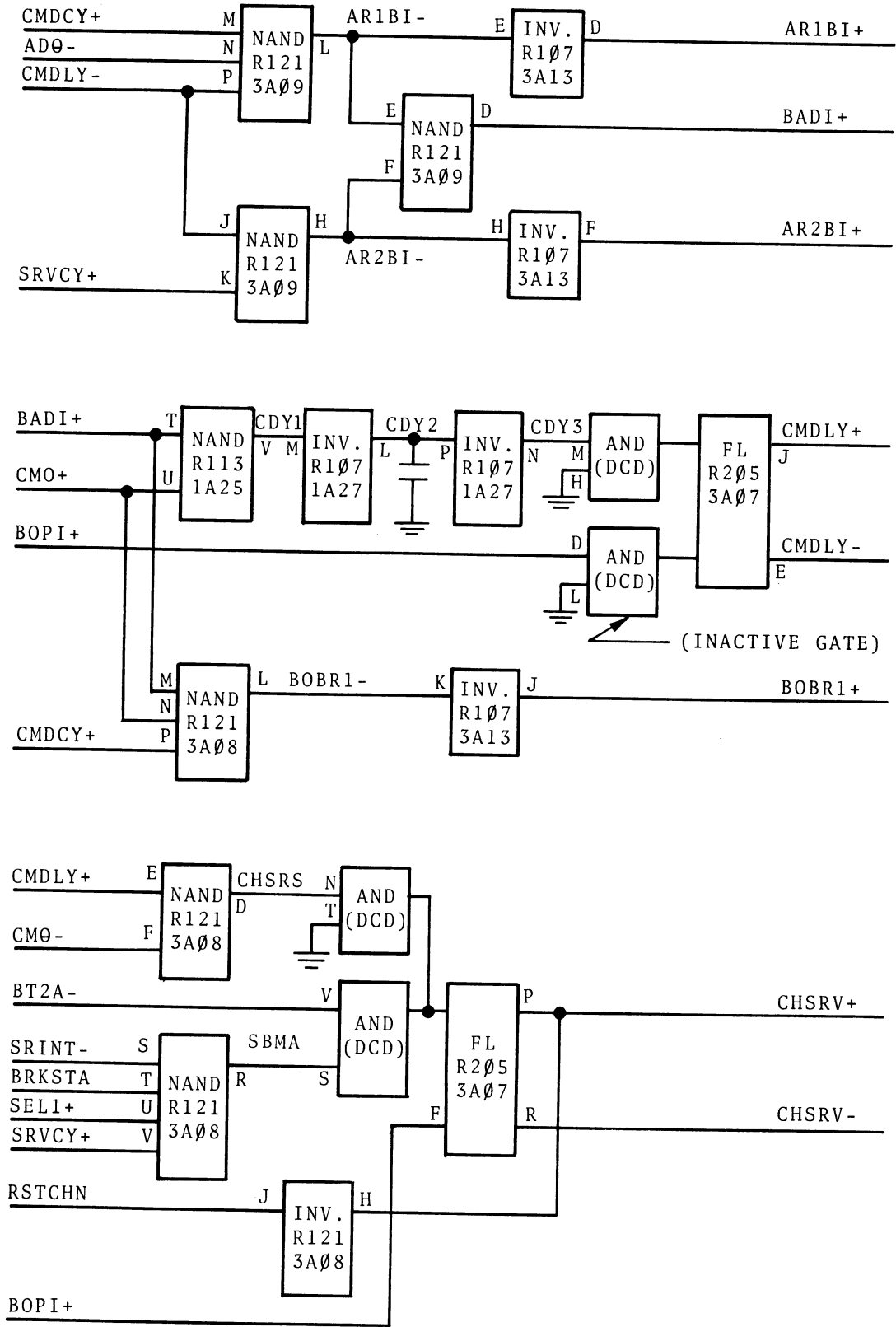
FIGURE E18.   COMMAND STORAGE
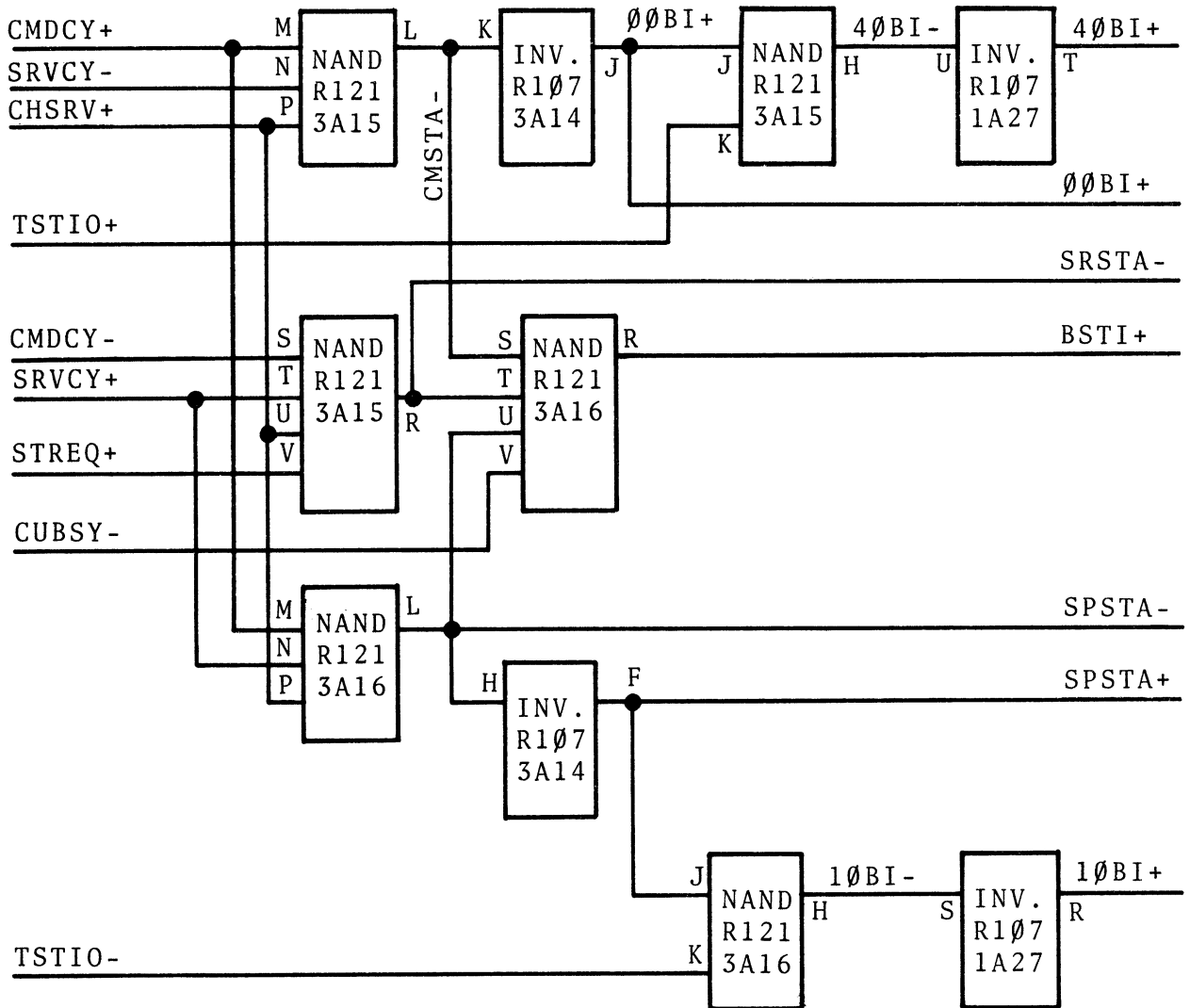
FIGURE E19. STATUS
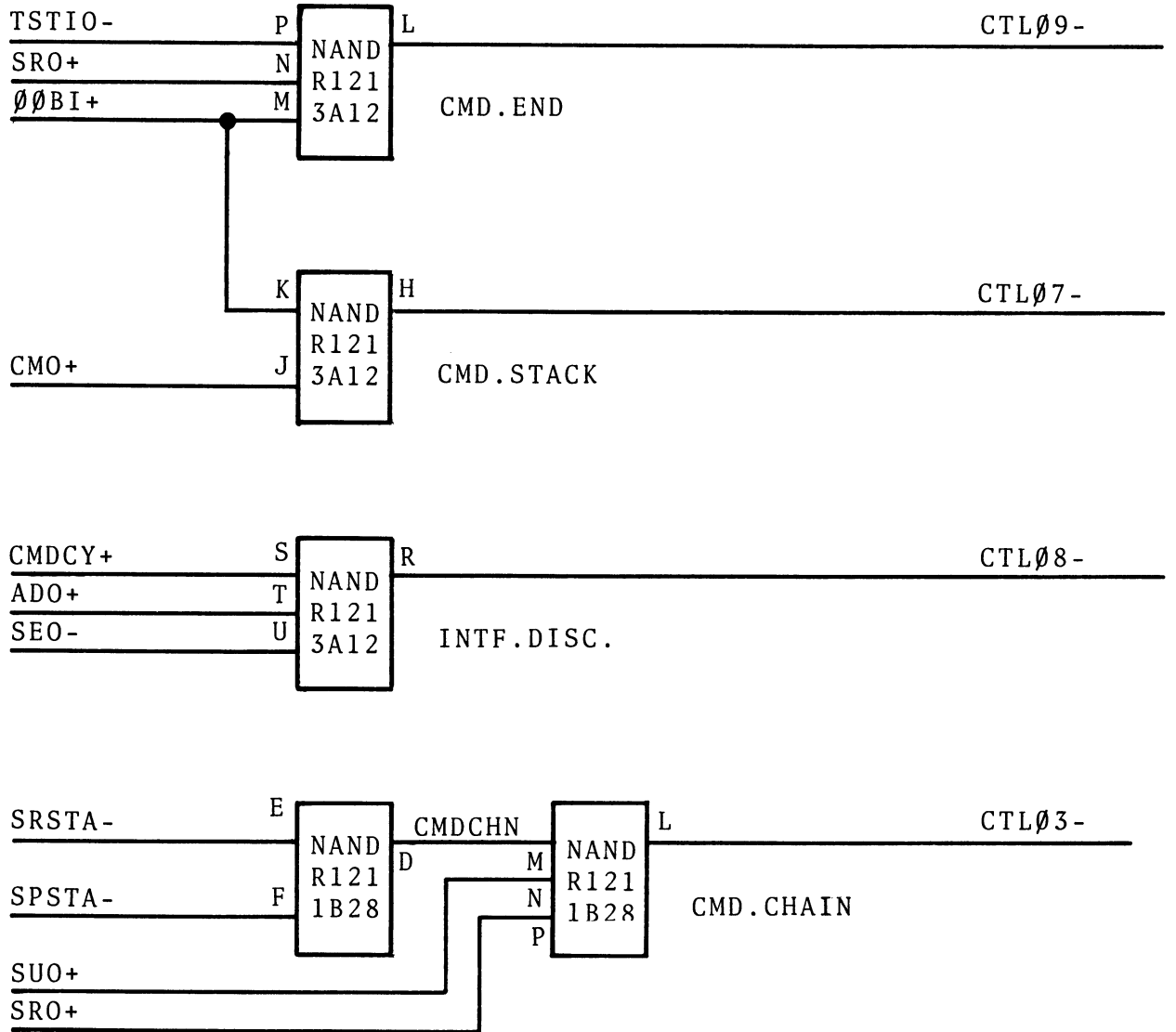
FIGURE E20. COMMAND CYCLE END.
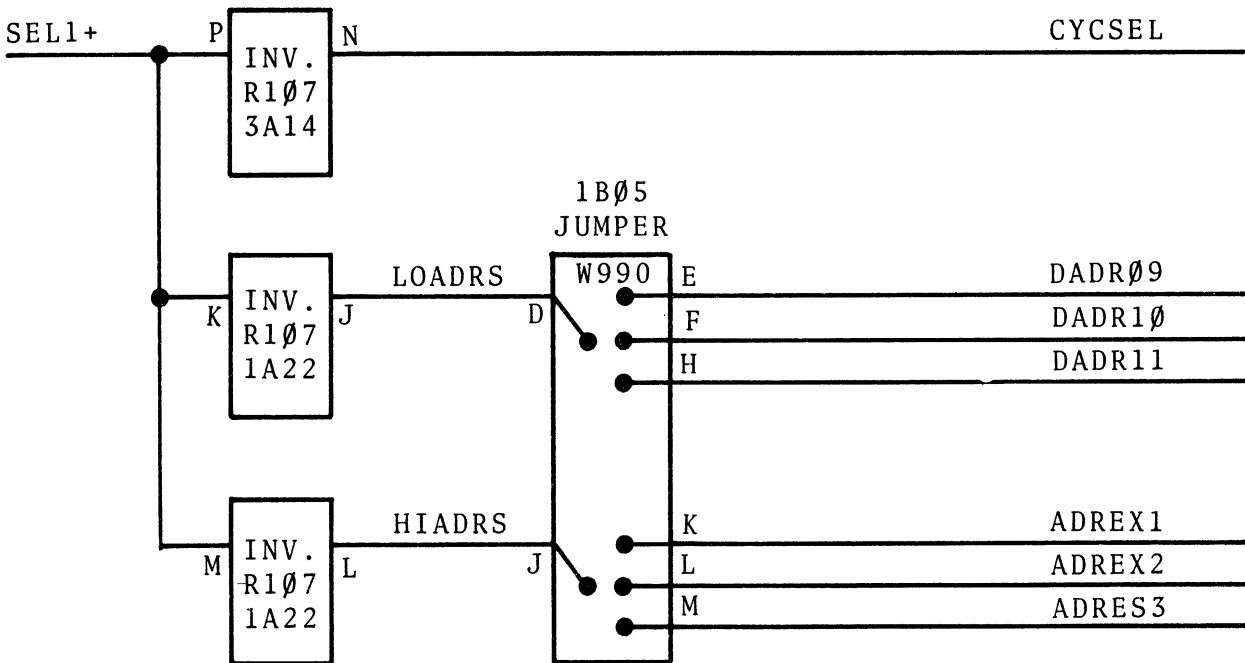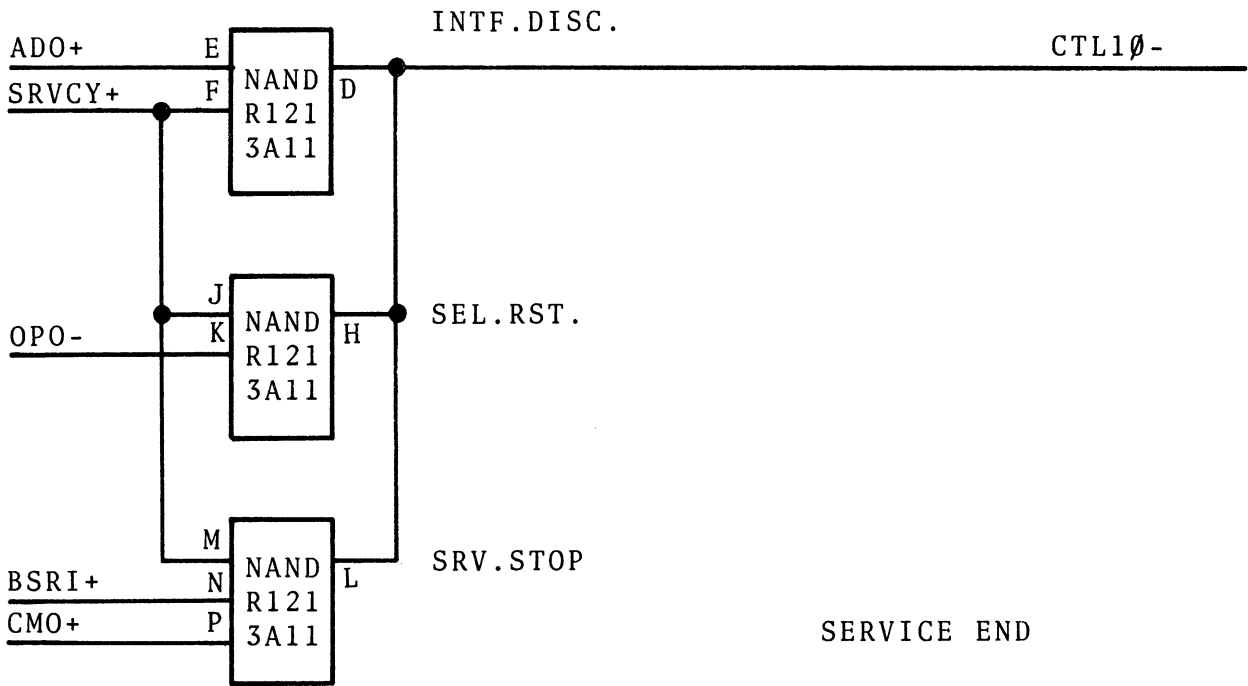
FIGURE E21. DATA BREAK
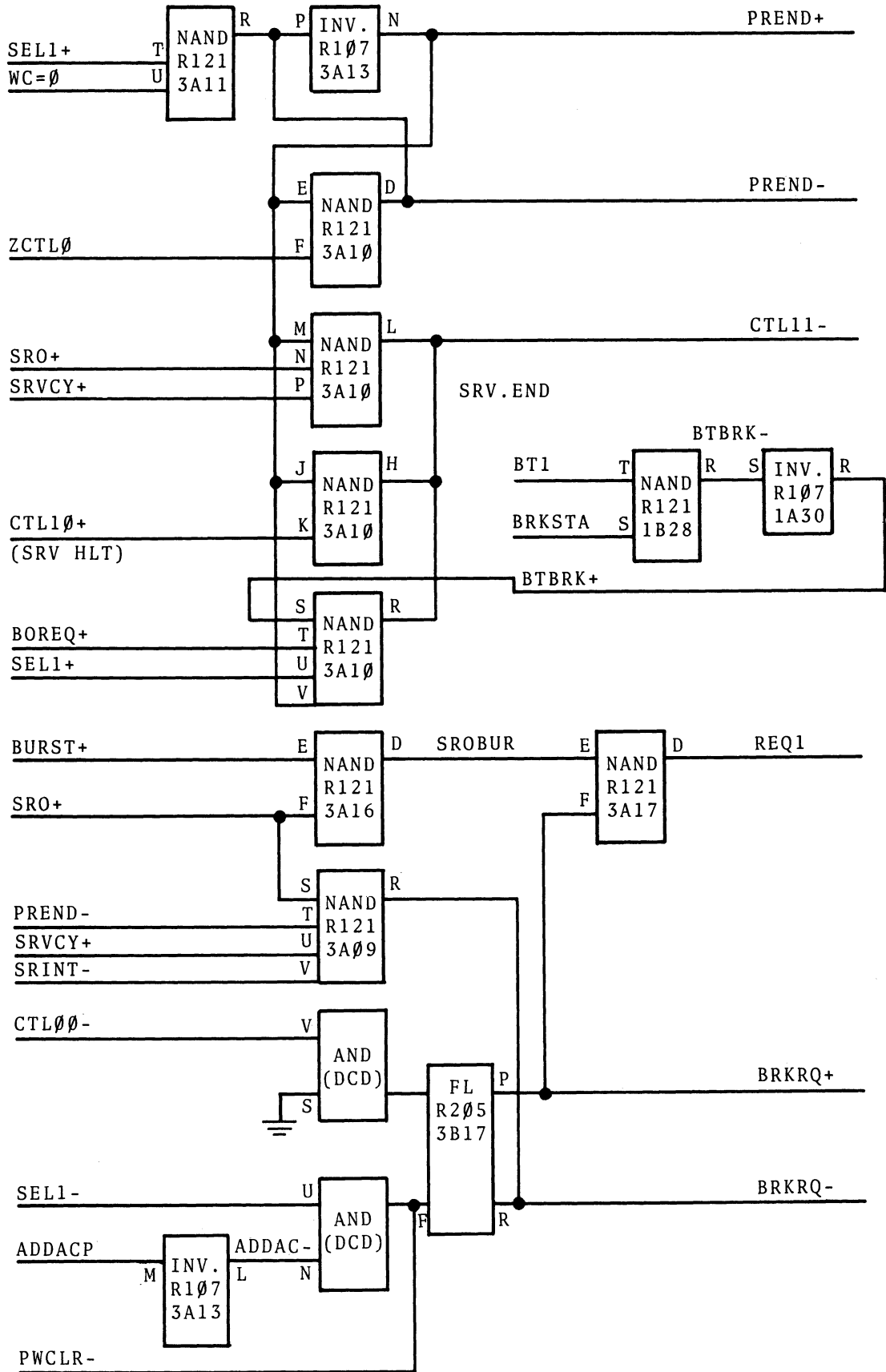
FIGURE E22. DATA BREAK.
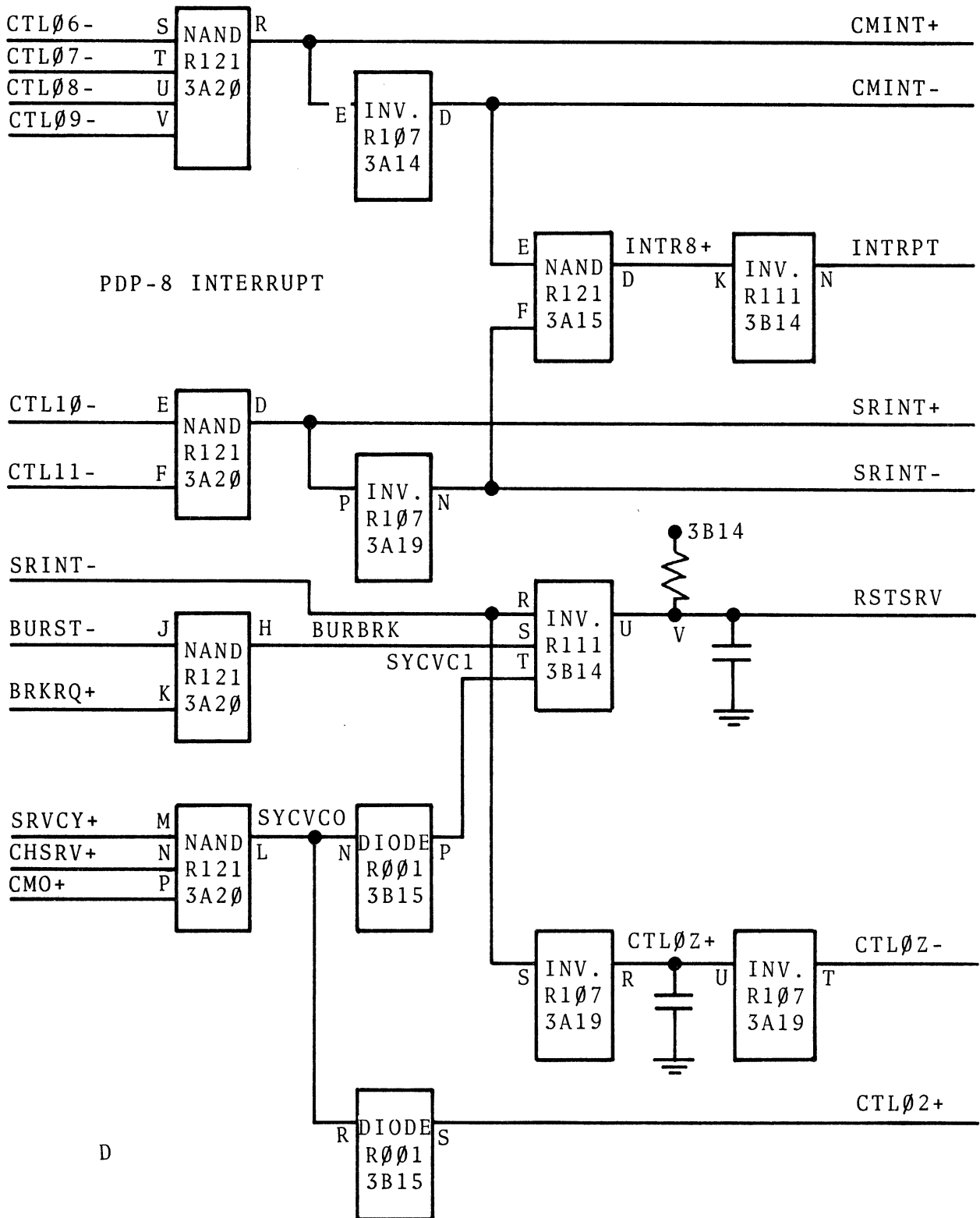
FIGURE E23.   SERVICE CYCLE RESET
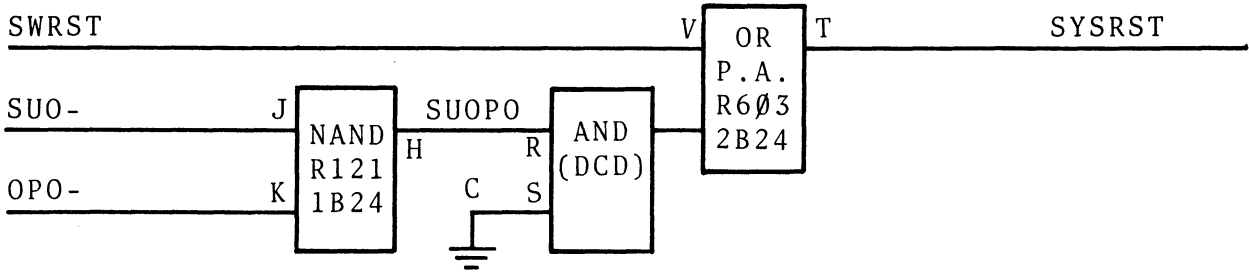
SYSTEM RESET
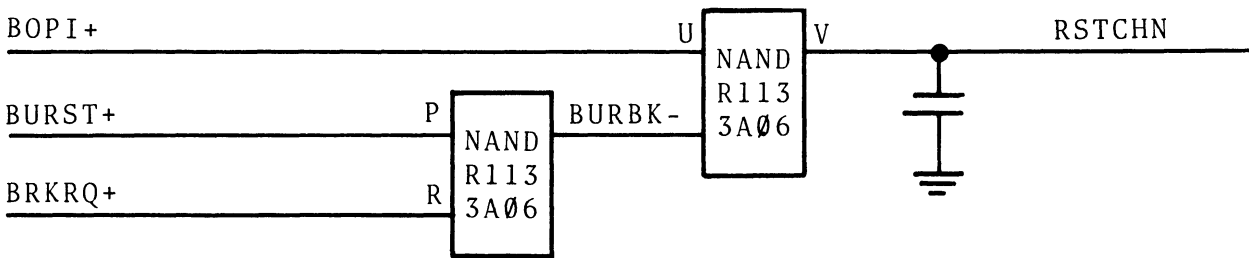
CHANNEL SERVICE RESET
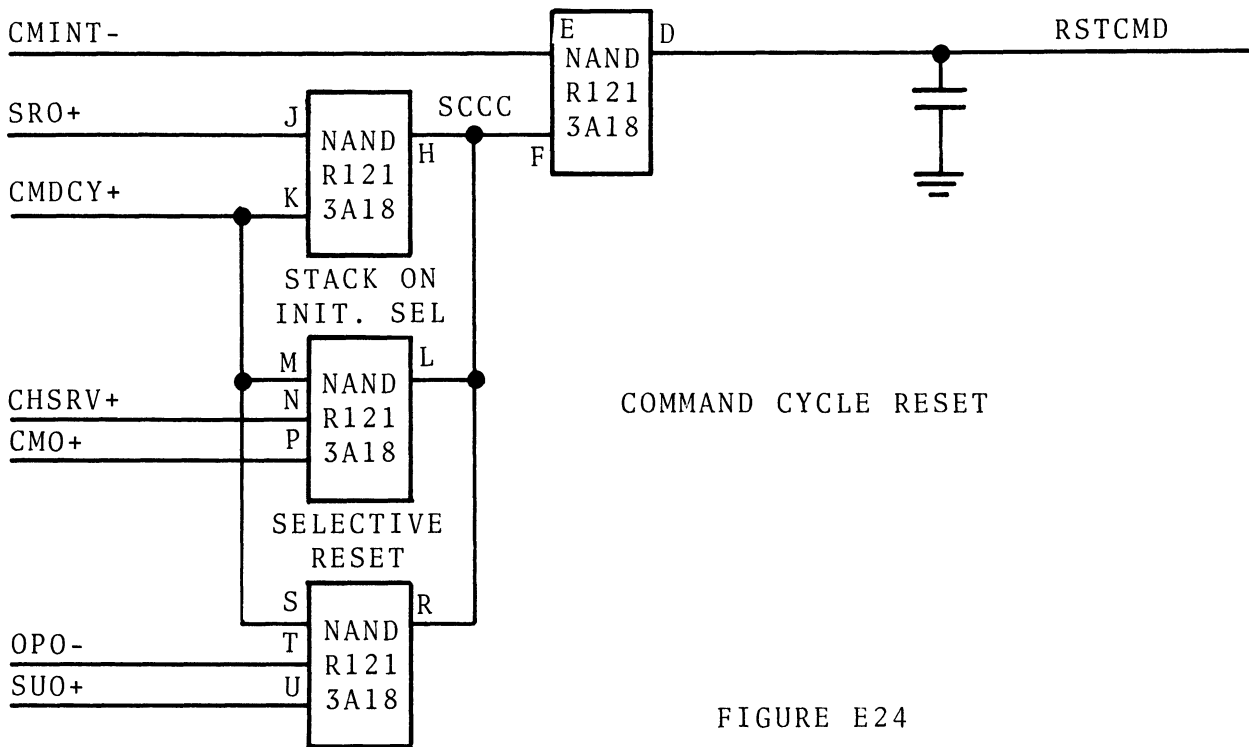
COMMAND CYCLE RESET

FIGURE E24
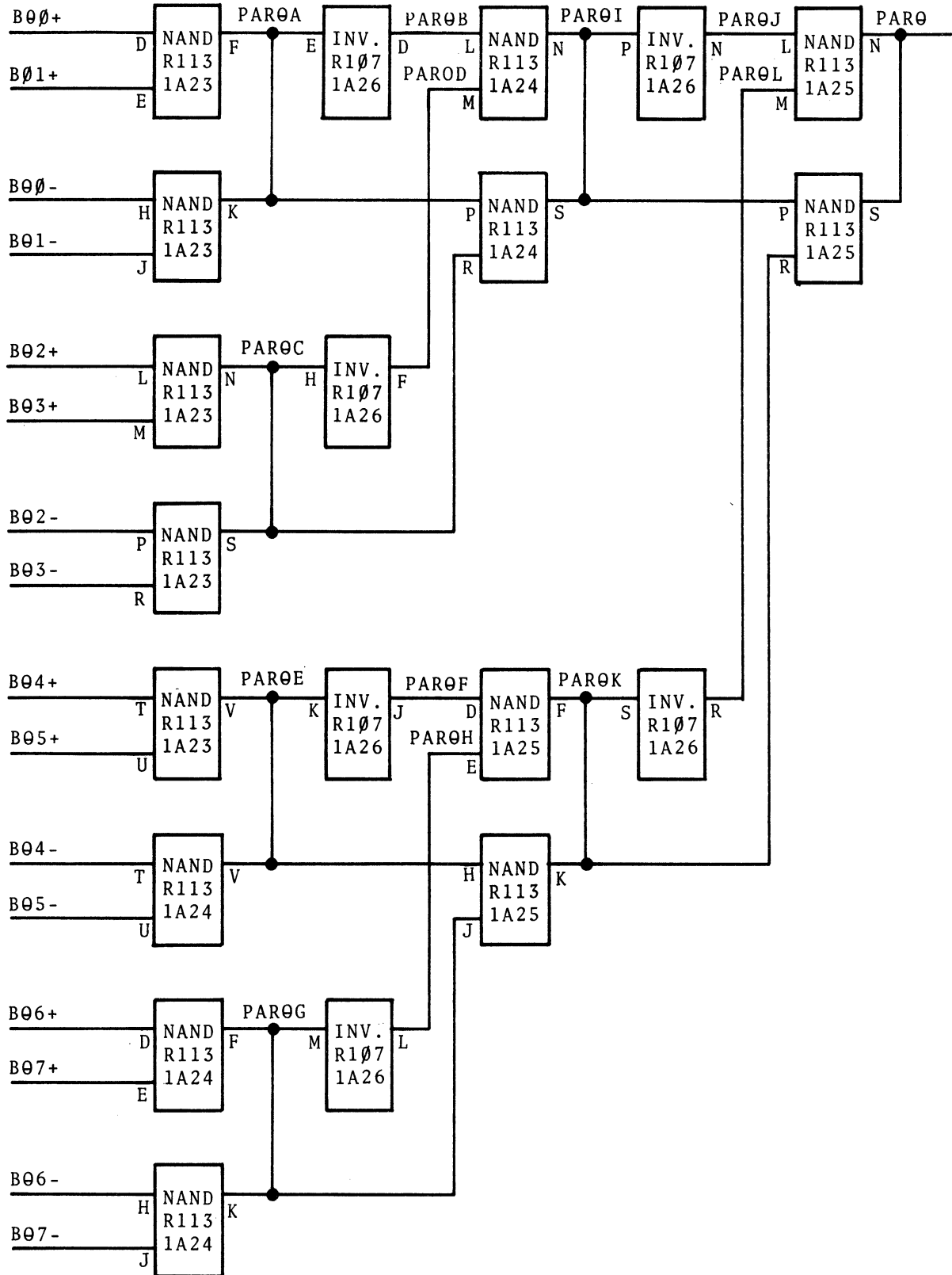
FIGURE E25. BUS OUT PARITY
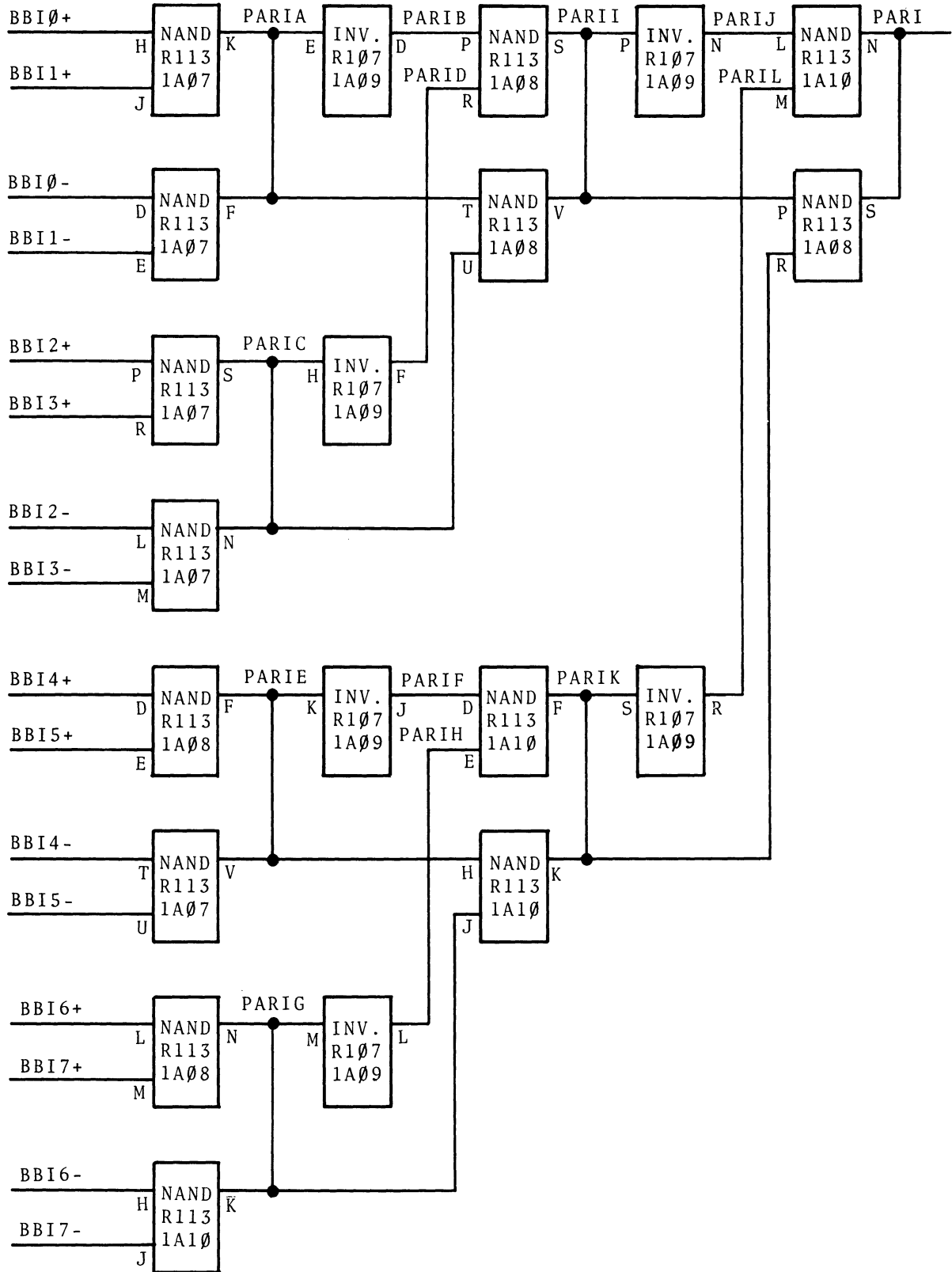
FIGURE E26. BUS IN PARITY

BUS OUT PARITY CHECK

BUS IN PARITY CHECK
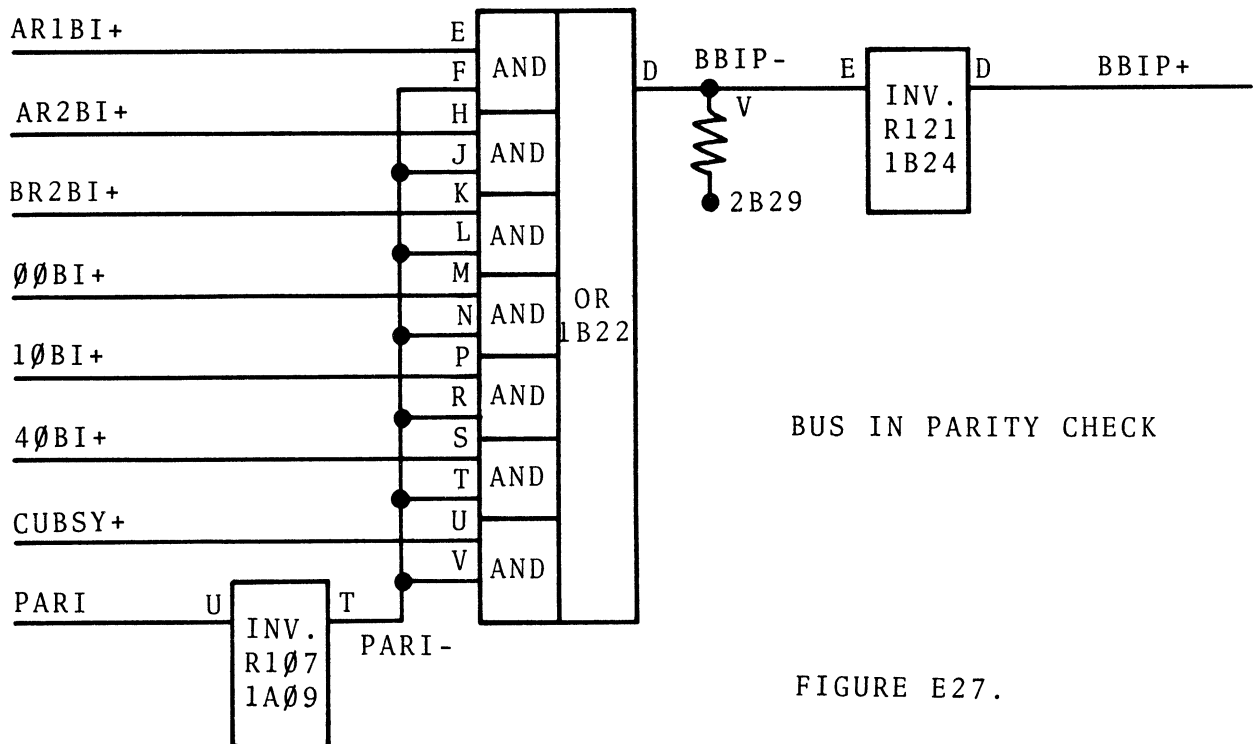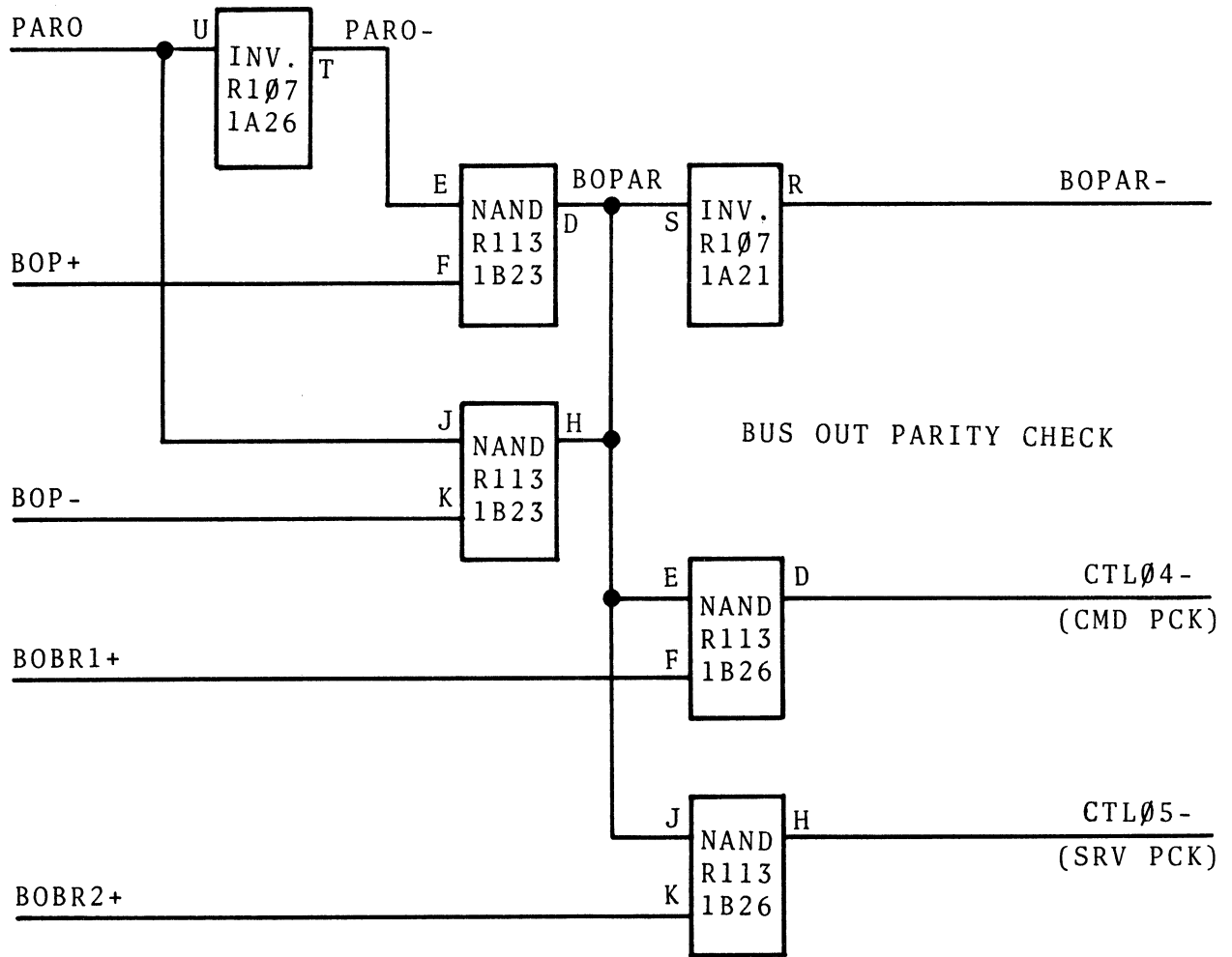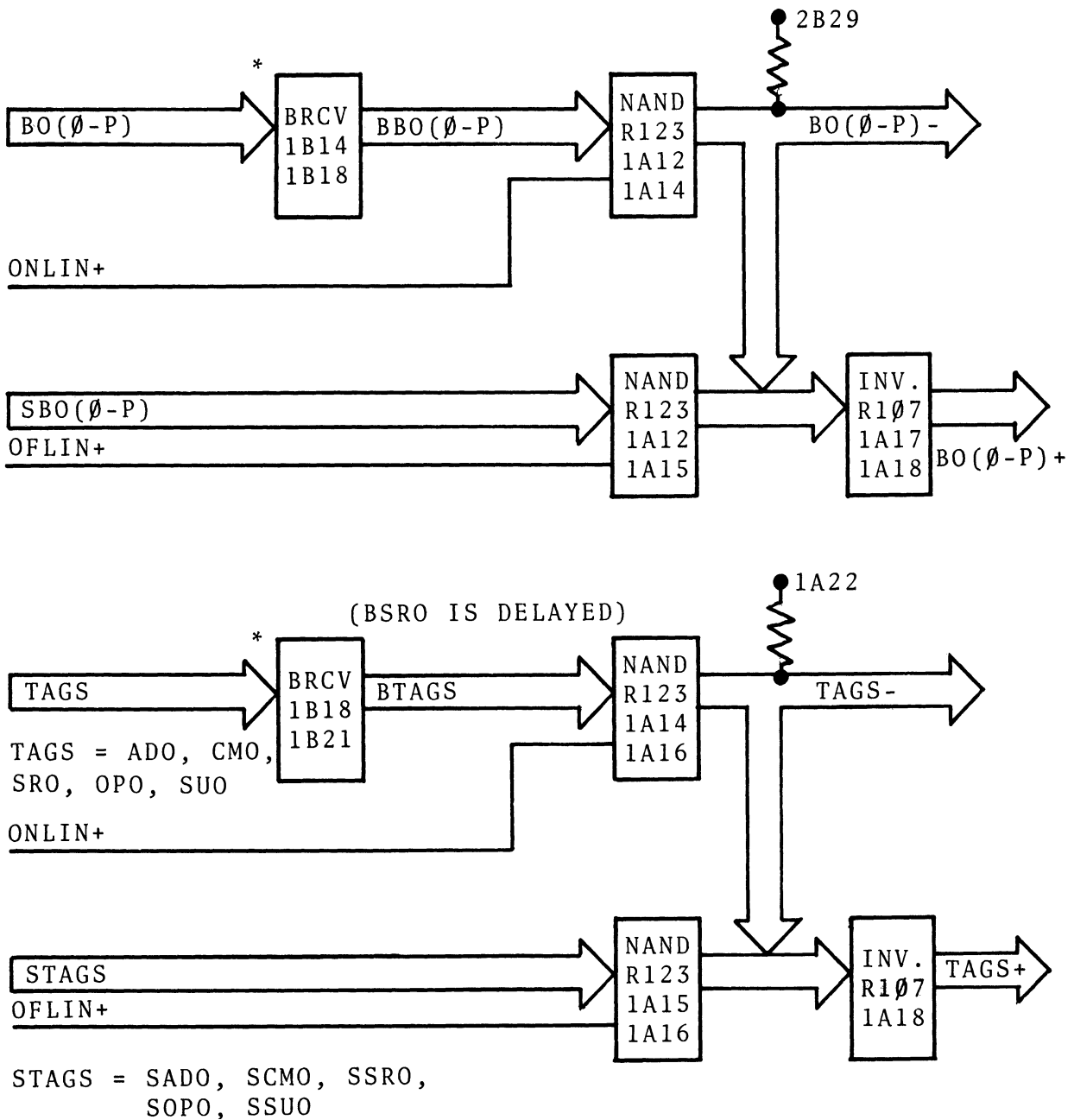
FIGURE E27.

FIGURE E28. BUS-TAGS OUT GATING
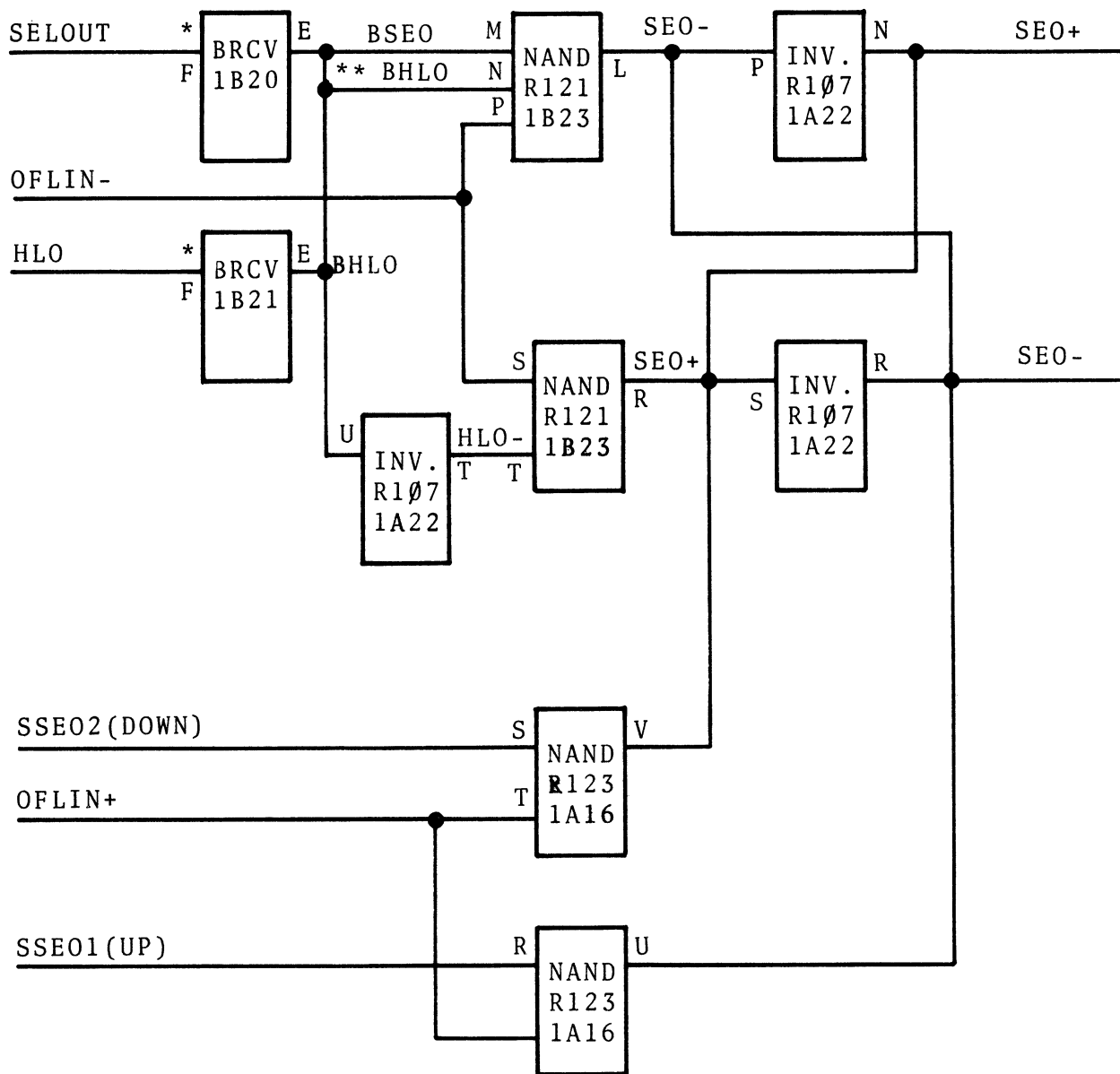
FIGURE E29.   SELECT OUT GATING

BBI(∅-P)+ → NAND BDRV 1B∅6 1B1∅ * → BI(∅-P)
ONLIN+

(TAGS) → NAND BDRV 1B1∅ 1B12 * → (TAGS)
BADI+   ADI
BSTI+   STI
BSRI+   SRI
BREI+ (NO DELAY)   REI
BOPI+   OPI

ONLIN+

SPROP+   F   BDRV   *   SELPRP
                    1B13 D
OFLIN-   H

                              *IBM LOGIC LEVELS

SELPRP
  (from relay)
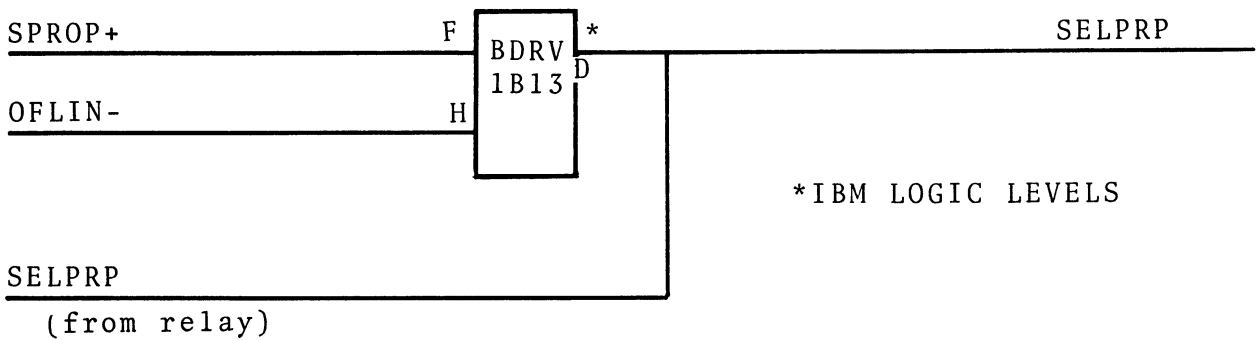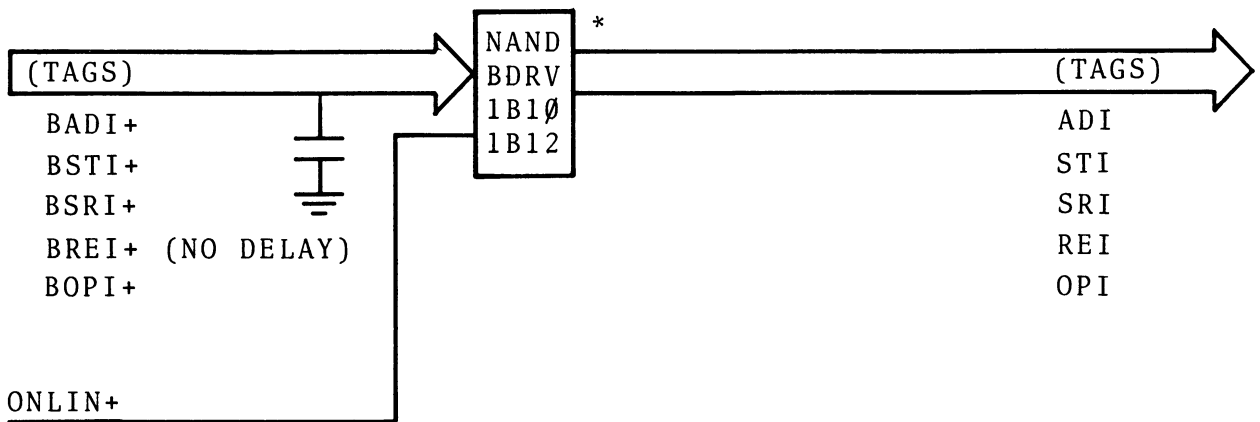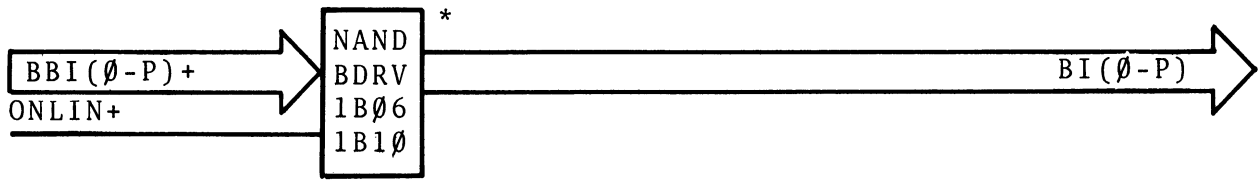
FIGURE E30.   BUS-TAGS IN GATING
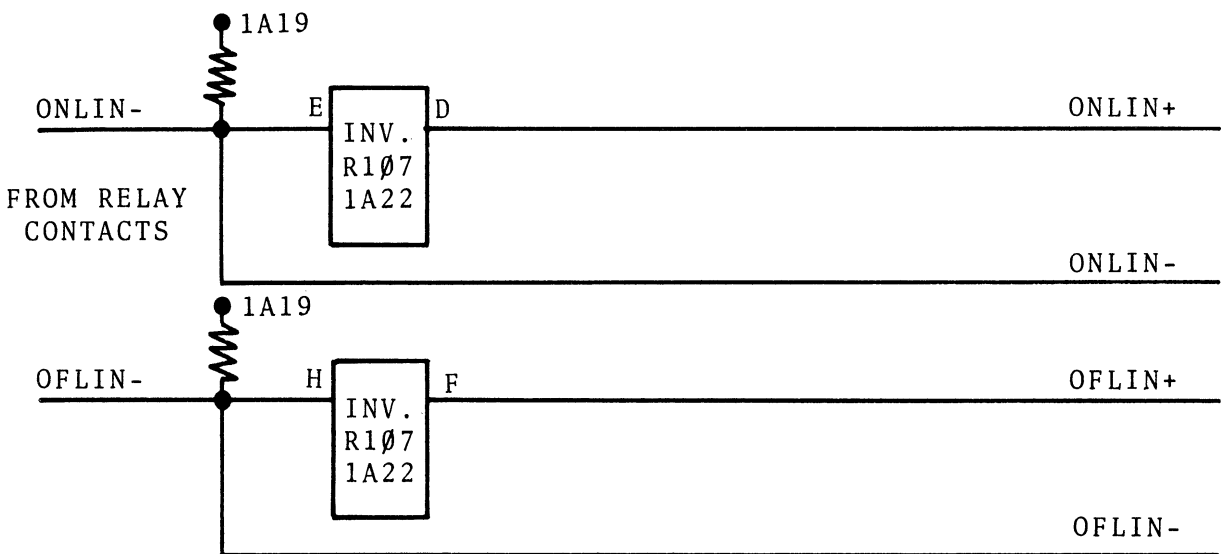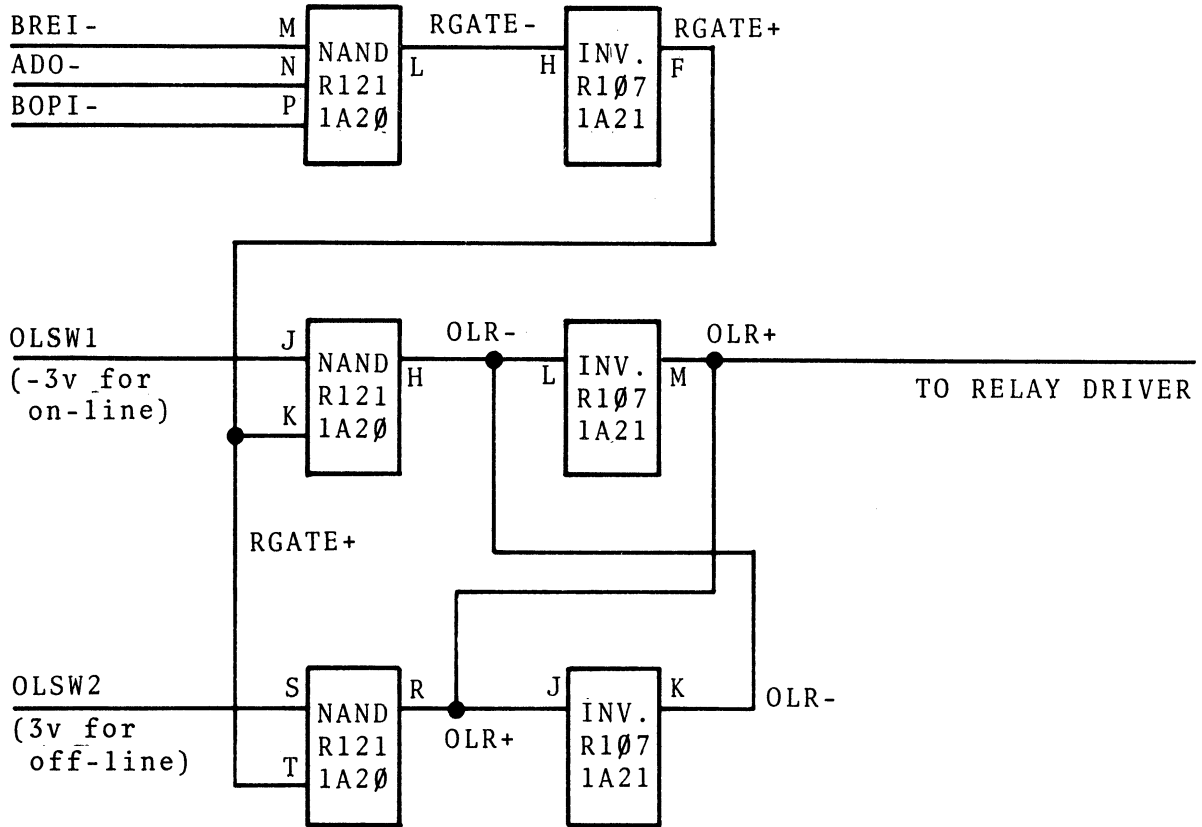
FIGURE E31.   ON-LINE/OFF-LINE CIRCUITRY
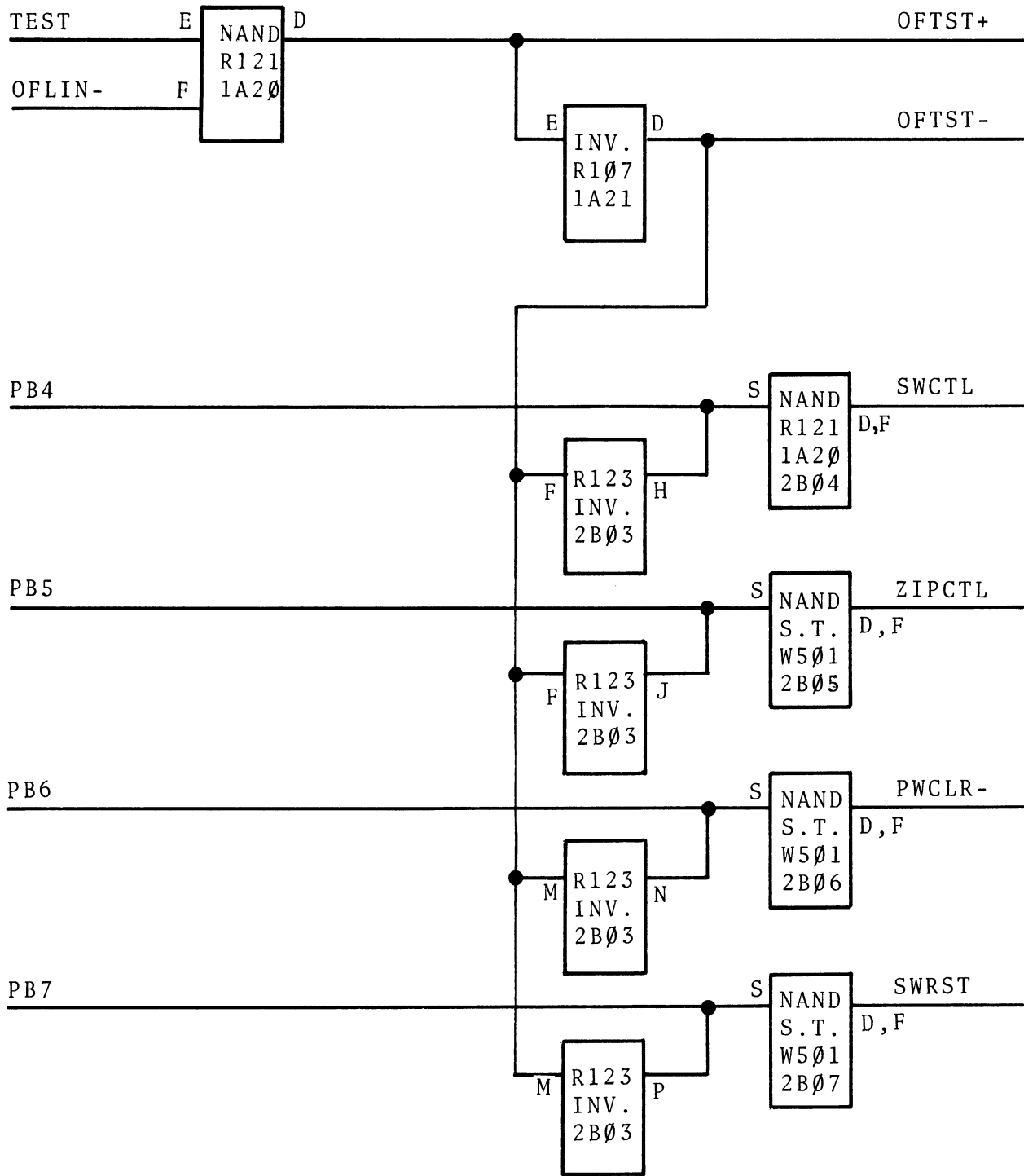
FIGURE E32. TEST PANEL PUSH BUTTON GATING

1 A	01-02 IBM BUS	03-04 PDP-8 PE03	05-06 PDP-8 ME30			31-32 IBM BUS
1 B	01-02 IBM TAG	03-04 PDP-8 PF03				31-32 IBM TAG
2 A	02 TEST PANEL PANEL	03 TEST PANEL PANEL		30 TEST PANEL PANEL	31 TEST PANEL PANEL	32 TEST PANEL PANEL
2 B	01 TEST PANEL PANEL	02 TEST PANEL PANEL		30 MPX	31 TEST PANEL PANEL	32 TEST PANEL PANEL
3 A	01-02 PDP-8 PE02	03-04 PDP-8 PE04		28 EAC	29-30 PDP-8 ME34	31-32 PDP-8 ME35
3 B	01-02 PDP-8 PF02	03-04 PDP-8 PF04		28 EAC	29-30 PDP-8 MF34	31-32 PDP-8 MF35

FIGURE E33. CONNECTOR POSITIONS

```
                                              D  AC∅∅
                                              E  AC∅1
    ┌──────────┐         ┌──────────┐         H  AC∅2
    │  CABLE   │         │ CABLE TO │         K  AC∅3
    │  FROM    │━━━━━━▶  │  PDP-8   │         M  AC∅4
    │ DEVICES  │         │  W∅21    │         P  AC∅5
    │  W∅21    │   ▲     │  3A∅1    │         S  AC∅6
    │  3A∅2    │   ┃     └──────────┘         T  AC∅7
    └──────────┘   ┃                          V  AC∅8
  ┌────────────┐   ┃
  │ AC(∅-8)    │───┘
  └────────────┘
```

CABLE FROM DEVICES W∅21 3B∅2

ACJ2

CABLE TO PDP-8 W∅21 3B∅1

V D E H K M P S T

ACCLR P
RUN S
ACJ1 T

AC∅9
AC1∅
AC11
SKIP
INTRPT
REQ1

CABLE TO MULTIPLEX W∅21 2B3∅

M
K
D
E

●3B∅8

SEL1-

S INV. R1∅7 3A14 R SEL1+

D DADR∅∅
E DADR∅1
H DADR∅2
K DADR∅3
M DADR∅4
P DADR∅5
S DADR∅6
T DADR∅7
V DADR∅8

CABLE DEVICES W∅21 1A∅4

DATA ADD(∅-8)

CABLE TO PDP-8 W∅21 1A∅3

CABLE FROM DEVICES W∅21 1B∅4

DAJ

BRKREQ

MBINCR

CABLE TO PDP-8 W∅21 1B∅3

V D E H K M P S T

DADR∅9
DADR1∅
DADR11
XFER

ADDACP
BRKSTA

FIGURE E34. PDP-8 CABLE CONNECTORS (Page 1 of 3)

FIGURE E34.   PDP-8 CABLE CONNECTORS (Page 2 of 3)

BBIP+	D
BBI0+	E
BBI1+	F
BBI2+	H
BBI3+	J
BBI4+	K
BBI5+	L
BBI6+	M
BBI7+	N
CTL00+	P
CTL01+	R
CTL02+	S
CTL03+	T
CTL04+	U
CTL05+	V

W021MJ CABLE TO TEST PANEL 2B31

(ISOLATORS ON ALL LINES)

BOP+	D
BO0+	E
BO1+	F
BO2+	H
BO3+	J
BO4+	K
BO5+	L
BO6+	M
BO7+	N
CTL06+	P
CTL07+	R
CTL08+	S
CTL09+	T
CTL10+	U
CTL11+	V

W021MJ CABLE TO TEST PANEL 2B32

(ISOLATORS ON ALL LINES)

(SWITCH FILTERS ON ALL LINES)

W021MJ CABLE TO TEST PANEL 2A30

SBOP
SBO0
SBO1
SBO2
SBO3
SBO4
SBO5
SBO6
SBO7

FIGURE E36. TEST PANEL CONNECTORS (Page 3 of 3)

D BIØ
E BI1
H BI2
K BI3
M BI4
P BI5
S BI6
T BI7
V BIP

BI(Ø-P)

WØ21 IBM CABLE 1AØ1

WØ21 IBM CABLE 1AØ2

BO(Ø-P)

WØ21 IBM CABLE 1A32

WØ21 IBM CABLE 1A31

D BOØ
E BO1
H BO2
K BO3
M BO4
P BO5
S BO6
T BO7
V BOP

FIGURE E35.   IBM CABLE CONNECTORS

(Page 1 of 2)

WØ21 IBM CABLE 1BØ1

D
E
H
K
M SEI
P
S
T
V

SELOUT
ADO
CMO
SUO

OPI
STI
ADI
SRI

SELPRP

WØ21 IBM CABLE 1BØ2

D
E
H
K
M
P
S
T
V

NOTE: ALL LINES CARRY IBM LOGIC LEVELS.

NOTE: ALL LINES CARRY IBM LOGIC LEVELS

FIGURE E35. IBM CABLE CONNECTORS(Page 2 of 2)
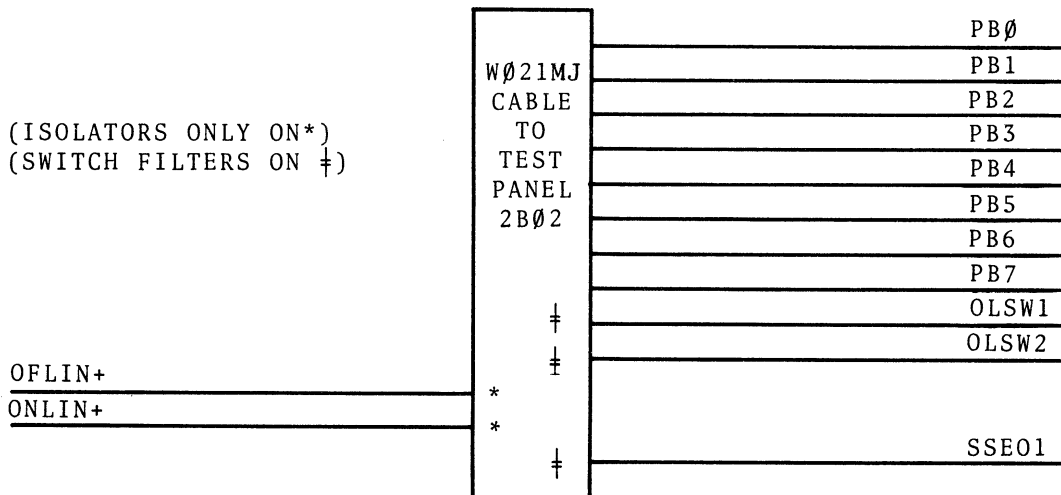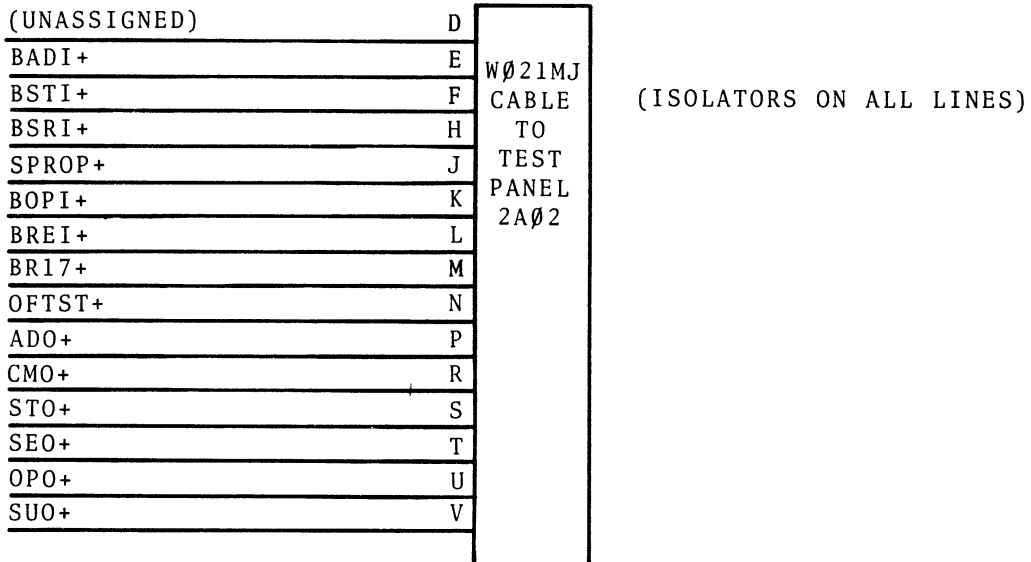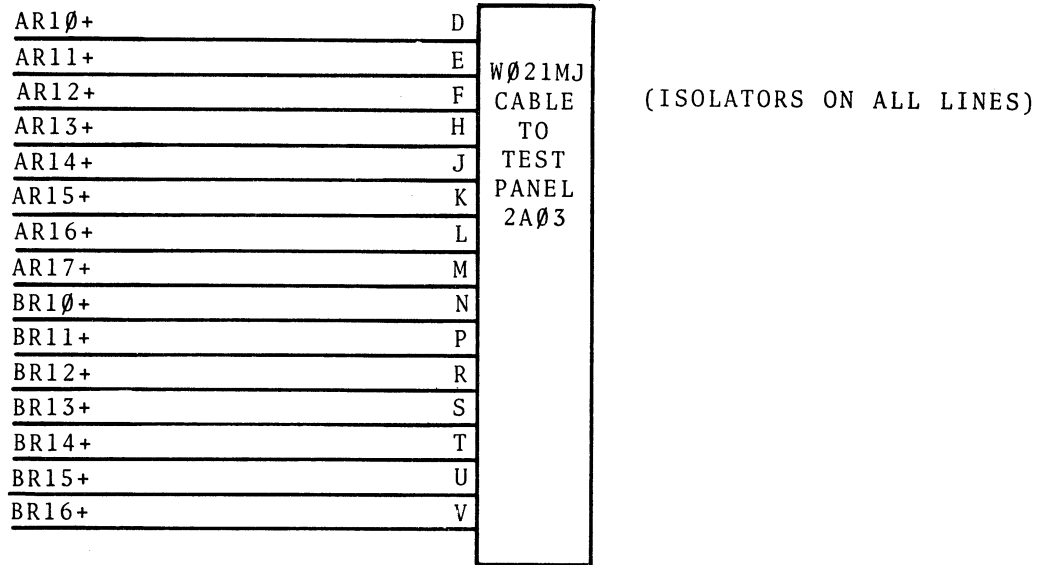
FIGURE E36.   TEST PANEL CONNECTORS (Page 1 of 3)

(SWITCH FILTERS
ON ALL LINES)

D		TEST
E		SADO
F		SCMO
H		SSRO
J		SSEO2
K		SOPO
L		SSUO
M		SWØ+
N		SW1+
P		SW2+
R		SW3+
S		SW4+
T		SW5+
U		SW6+
V		SW7+

WØ21MJ CABLE TO TEST PANEL 2BØ1

AR2Ø+	D
AR21+	E
AR22+	F
AR23+	H
AR24+	J
AR25+	K
AR26+	L
AR27+	M
SEL+	N
CMDCY+	P
SRVCY+	R
CUBSY+	S
CMDLY+	T
CHSRV+	U

WØ21MJ CABLE TO TEST PANEL 2A31

(ISOLATORS ON ALL LINES)

BR2Ø+	D
BR21+	E
BR22+	F
BR23+	H
BR24+	J
BR25+	K
BR26+	L
BR27+	M
CHNRQ+	N
PREND+	P
BRKRQ+	R
INTR8+	S
SKIP+	T
EACENB	U

WØ21MJ CABLE TO TEST PANEL 2A32

(ISOLATORS ON ALL LINES)

FIGURE E36. TEST PANEL CONNECTORS (Page 2 of 3)

-141-
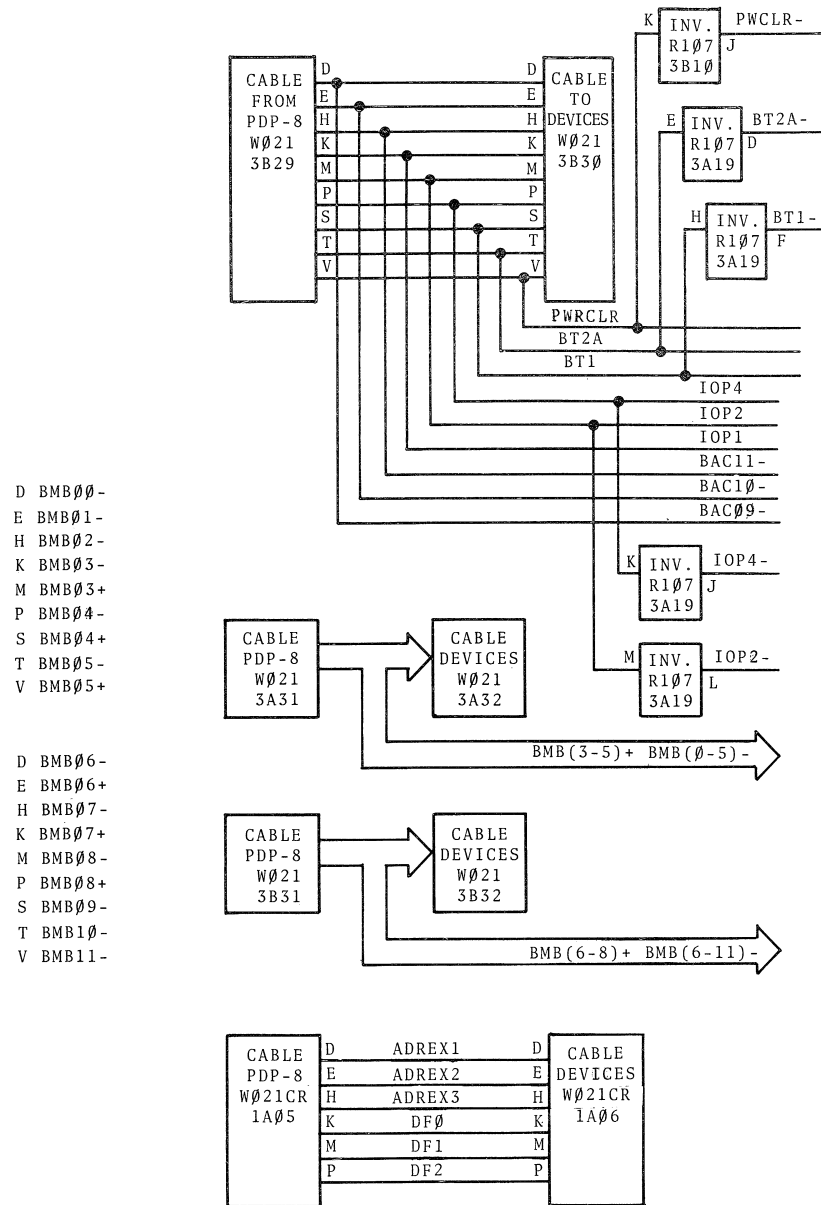
FIGURE E34. PDP-8 CABLE CONNECTORS (Page 3 of 3)

PANEL 1 ... IBM INTERFACE ... BUSS DRIVERS AND RECEIVERS

Panel A

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
	W021CR	W021CR	W021CR	W021CR	W021CR	W021CR	R113	R113	R107	R113	R107	R123	R123	R123	R123	R123	R107	R107	W002	R121	R107	R107	R113	R113	R113	R107	R107	W501	W501	R107	W021CR	W021CR
C	GN1A01																															
D	BIO	BIO	DADR00	DADR00	ADREX1	ADREX1	BBIO-	BBI4+	*PARIB	PARIF	*BBIO+	BB00	BB04	BB06	BCMO	BOPO	*B00+	*B07+	BOP-	*OFTST+	*OFTST-	*ONLIN+	B00+	B06+	PAROF	*PAROB	*BBI7+	SCMO+	SSRO+	*	B00	B00
E	BI1	BI1	DADR01	DADR01	ADREX2	ADREX2	BBI1-	BBI5+	PARIA	PARIH	BBIO-	BB01	BB05	BB07	BSRO	BSUO	B00-	B07-	ADO-	TEST	OFTST+	ONLIN-	B01+	B07+	PAROH	PAROA	BBI7-				B01	B01
F	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	*PARIA	*PARIE	*PARID	*PARIK	*BBI1+	ONLIN+	ONLIN+	ONLIN+	ONLIN+	ONLIN+	*B01+	*BOP+	SRO-	OFLIN-	*RGATE+	*OFLIN+	*PAROA	*PAROG	*PAROK	*PAROD	BBI7-				GN1A31	GN1A31
H	BI2	BI2	DADR02	DADR02	ADREX3	ADREX3	BBI0+	BBI6-	PARIC	PARIE	BBI1-	*B00-	*B04-	*B06-	*CMO-	*OPO-	B01-	BOP-	MB04	*OLR-	RGATE-	OFLIN-	B00-	B06-	*PAROE	*PAROC	BREI-	*SCMO+	*SSRO+	*	B02	B02
J	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	BBI1+	BBI7-	*PARIF	PARIG	*BBI2+	*B01-	*B05-	*B07-	*SRO-	*SUO-	*B02+	*ADO+	MB05	OLSW1	*OLR+	*LOADRS	B01-	B07-	PAROG	*PAROF	*SPROP+				GN1A31	GN1A31
K	BI3	BI3	DADR03	DADR03	DF0	DF0	*PARIA	*PARIG	PARIE	PARIJ	*BBI3+	SB00	SB04	SB06	SCMO+	SOPO	*B02-	ADO-	MB06	RGATE+	*OLR-	SEL1+	*PAROA	*PAROG	*PAROK	PAROE	SPROP-	PB092	PB102	BOPI+	B03	B03
L	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	BBI2-	BBI6+	*PARIH	PARIJ	*BBI3+	SB01	SB05	SB07	SSRO+	SSUO	*B03+	*CMO+	MB07	*RGATE-	*OLR-	*HIADRS	B02+	*PAROB	PAROJ	*PAROH	*SKIP+	PB092	PB102	*SKIP-	GN1A31	GN1A31
M	BI4	BI4	DADR04	DADR04	DF1	DF1	BBI3-	BBI7+	PARIG	PARIL	BBI3-	OFLIN+	OFLIN+	OFLIN+	OFLIN+	OFLIN+	B03-	CMO-	MB08	BREI-	OLR+	SEL1+	B03+	*PAROD	PAROL	*PAROG	CDY1	PB093	PB103	CDY1	B04	B04
N	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	*PARIC	*PARIG	*PARIJ	*PARI	*BBI4+	*B00-	*B04-	*B06-	*CMO-	*OPO-	*B04+	*SRO+	MB09	ADO-	*BDGATE	*SEO+	*PAROC	*PAROI	*PARO	*PAROJ	*CDY3	PB093	PB103	*SRVENB	GN1A31	GN1A31
P	BI5	BI5	DADR05	DADR05	DF2	DF2	BBI3+	PARID	PARII	PARIK	*BBI5+	BB02	SB02	BB0P	SB0P	SSE01	*B05+	*B04-	MB10	BOPI+	ONLIN-	SEO-	B02-	*PAROA	PAROI	PAROI	CDY2				B05	B05
R	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	*PARIC	PARID	PARIL	PARIK	*BBI5+	BB02	SB02	BB0P	SB0P	SSE01	B05+	*B04-	MB11	ONLIN-		SEO-	B02-	*PARCA	PAROI	PAROI	CDY2			ADO+	B05	B05
S	BI6	BI6	DADR06	DADR06	AXJ1	AXJ1	*PARIC	*PARII	PARIK	PARI	BBI5-	BB03	SB03	BAD0	SAD0	SSE02	B05-	OPO-	OPO-	OLSW2	BOPAR	SEO+	*PAROC	*PAROC	PAROK	*PAROI	10BI-	PB091	PB101	*BTBRK+	GN1A31	GN1A31
T	BI7	BI7	DADR07	DADR07	AXJ2	AXJ2	BBI4-	PARIA	PARI		*BBI6+	ONLIN+	OFLIN+	ONLIN+	OFLIN+	OFLIN+	*B06+	*SUO+	SUO-	RGATE+	*PWCLR-	*HLO-	B04+	304-	BADI+	*PARO-	*40BI+	PB091	PB101	BTBRK-	B06	B06
U	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	GN1A01	BBI5-	PARIC	PARI		BBI6-	*B02-	*B02-	*BOP-	*BOP-	*SEO-	B06-	SUO-	ONLIN-		PWCLR-	BHLO	B05+	B05-	CMO+	PARO	*	SCMO	SSRO	*	GN1A31	GN1A31
V	BIP	BIP	DADR08	DADR08	AXJ3	AXJ3	*PARIE	*PARII		*		*B03-	*B03-	*AD0-	*AD0-	*SEO+	*B03-	*B03-	OFLIN-			OFLIN-	*PAROE	*PAROE	*CDY1						BOP	BOP

Panel B

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
	W021CR	W021CR	W021CR	W021CR	W990	BD	BD	BD	BD	BD	BD	BD	BD	BR	BR	BR	BR	BR	BR	BR	BR	R141	R121	R121	R121	R121	R107	R121	R151	W990	W021CR	W021CR
C	GN1B01																												GN1B29			
D	OPI	OPI	DADR09	DADR09	LOADRS	*BIO	*BI2	*BI4	*BI6	*BIP	*STI	*REI	*SELPRP									*BBIP-	*BOPAR	*BBIP+	*BOBR2+	*CTL04-	*BBI1-	*CMDCHN	GN1B29		SRO	SRO
E	STI	STI	DADR10	DADR10	DADR09									*BB00	*BB02	*BB04	*BB06	*BB0P	*BCMO	*BSE0	*BHLO	AR1BI+	PARO-	BBIP-	BOBR2-	BOPAR	40BI+	SRSTA-	GN1B29		CLO	CLO
F	GN1B01	GN1B01	DADR11	DADR11	DADR09	BBI0+	BBI2+	BBI4+	BBI6+	BBIP+	BSTI+	BREI+	SPROP+	B00	B02	B04	B06	B0P	CMO	SELOUT	HLO	PARI-	BOP+			BOBR1+	*BBI1-	SPSTA-	B01+	001F	GN1B31	GN1B31
H	ADI	ADI	DADR11	DADR11	DADR11	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE	B00	B02	B04	B06	B0P	CMO	SELOUT	HLO	AR2BI+	BOP+			BOBR1+	*BBI1-	SPSTA-	B01+	203F	GN1B31	GN1B31
J	GN1B01	GN1B01	GN1B01	GN1B01	HIADRS																	AR2BI+	*BOPAR	*SUOPO	*BSRI+	*BOPAR	CUBSY+	*SKIP+	B00+	405F	MTRO	MTRO
K	SRI	SRI	BRKREQ	BRKREQ	ADREX1																	PARI-	PARO	SUO-	SCCSBI	BOPAR	CTL5KP	*BBI2-	B00-	607F	GN1B31	GN1B31
L	GN1B01	GN1B01	GN1B01	GN1B01	ADREX2																	AR2BI+	BOP-	OPO-	SCCSBO	BOBR2+	CUBSY+	ACTEST	B00-	809F	MTRI	MTRI
M	SEI	SEI	XFER	XFER	ADREX3	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE	BDGATE										BR2BI+	*SEO-	*SCCSBI	*SCCSBO	BOBR2-	*BBI3-	*CTL03-	B02+	A0BF	GN1B31	GN1B31
N	GN1B01	GN1B01	GN1B01	GN1B01		BBI1+	BBI3+	BBI5+	BBI7+	BADI+	BSRI+	BOPI+		B01	B03	B05	B07	ADO	SRO	OPO	SUO	00BI+	BSEO	SRVCY+	SRVCY+	BSRI+	CUBSY+	CMDCHN	*001F	C0DF	REI	REI
P	SELOUT	SELPRP	BRKSTA	BRKSTA										*BB01	*BB03	*BB05	*BB07	*BAD0	*BSRO	*BOP0	*BSUO	PARI-	CHSRV+	CHSRV+	BOREQ+	BOREQ+	10BI+	SUO-	*203F	E0FF	GN1B31	GN1B31
R	GN1B01	GN1B01	GN1B01	GN1B01										B01	B03	B05	B07	AD0	SR0	OP0	SU0	10BI+	OFLIN-	BIREQ+	BOREQ+	BOREQ+	10BI+	SR0+	*405F	IBMJ	IBMJ
S	ADO	AD0	ADDACP	ADDACP																		PARI-	*SEO+	*BR2BI+	*ZBR2	*BRKST-	*ADRDT-	*BTBRK-	*607F	GN1B31	GN1B31
T	CMO	CMO	MBINCR	MBINCR		*BI1	*BI3	*BI5	*BI7	*ADI	*SRI	*OPI	*									40BI+	OFLIN-	SCCSBO	SRVCY+	CTL00-	ADRDT-	BRKSTA	*809F	PWRINT	PWRINT
U	GN1B01	GN1B01	GN1B01	GN1B01																		PARI-	HL0-	SRSTA-	BOREQ+	BRKSTA	*BOPI-	BT1	*A0BF	HL0	HL0
V	SUO	SUO	DAJ	DAJ																		CUBSY+		SPSTA-	CHSRV+	SEL1+	BOPI+		*C0DF	GN1B31	GN1B31
																						PARI-							*E0FF		OPO	OPO

PANEL 2 ... ADDRESS AND BUFFER REGISTERS

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
	RELAY	W028S	W028S	W501	W501	W501	W501	R603	R205	R205	R205	R205	R205	R205	R205	R205	R141	R141	R141	R205	R205	R205	R205	R603	R205	R205	R205	R205	R107	W028S	W028S	W028S	
A																																	A
B																																	B
C	G2A01		GOD														GN2A17																C
D		AR10+	GOD	SWAR1	SWBR1	SWAR2	SWBR2	IOP2-	PSWAR1	PSWAR1	PSWAR1	PSWAR1	PSWBR1	PSWBR1	PSWBR1	PSWBR1	*AR=AR	*AR=AR	*AR=AR	PSWAR2	PSWAR2	PSWAR2	PSWAR2	IOP2-	PSWBR2	PSWBR2	PSWBR2	PSWBR2	*SW0-	SB0P	AR20+	BR20+	D
E		AR11+	BADI+					*AR1AC-	*AR10-	*AR11-	*AR12-	*AR13-	*BR10-	*BR11-	*BR12-	*BR13-	AR10+	AR12+	AR15+	*AR20-	*AR21-	*AR22-	*AR23-	*AR2AC-	*BR20-	*BR21-	*BR22-	*BR23-	SW0+	SB00	AR21+	BR21+	E
F	SELOUT	AR12+	BSTI+	*SWAR1	*SWBR1	*SWAR2	*SWBR2	PDCAR1	PDCAR1	PDCAR1	PDCAR1	PDCBR1	PDCBR1	PDCBR1	PDCBR1	PDCBR1	AR20-	AR22+	AR25+	PDCAR2	PDCAR2	PDCAR2	PDCAR2	PDCAR2	PDCBR2	PDCBR2	PDCBR2	PDCBR2	*SW1-	SB01	AR22+	BR22+	F
H		AR13+	BSRI+						BAC04-	BAC05-	BAC06-	BAC07-	BAC04-	BAC05-	BAC06-	BAC07-	AR10-	AR12+	AR15+	BAC04-	BAC05-	BAC06-	BAC07-		BMB04-	BMB05-	BMB06-	BMB07-	SW1+	SB02	AR23+	BR23+	H
J	OFLIN-	AR14+	SPROP+					PWCLR-	*AR10+	*AR11+	*AR12+	*AR13+	*BR10+	*BR11+	*BR12+	*BR13+	AR20+	AR22+	AR25+	*AR20+	*AR21+	*AR22+	*AR23+	PWCLR-	*BR20+	*BR21+	*BR22+	*BR23+	*SW2-	SB03	AR24+	BR24+	J
K		AR15+	BOPI+	PB02	PB12	PB22	PB32	SWAR1	SW0-	SW1-	SW2-	SW3-	SW0-	SW1-	SW2-	SW3-	AR11+	AR13+	AR16+	SW0-	SW1-	SW2-	SW3-	SWAR2	SW0-	SW1-	SW2-	SW3-	SW2+	SB04	AR25+	BR25+	K
L	ONLIN-	AR16+	BREI+	PB02	PB12	PB22	PB32	OFTST-	SW0+	SW1+	SW2+	SW3+	SW0+	SW1+	SW2+	SW3+	AR21-	AR23-	AR26-	SW0+	SW1+	SW2+	SW3+	OFTST-	SW0+	SW1+	SW2+	SW3+	*SW3-	SB05	AR26+	BR26+	L
M		AR17+	BR17+	PB03	PB13	PB23	PB33	*PSWAR1	PACAR1	PACAR1	PACAR1	PACAR1	PACBR1	PACBR1	PACBR1	PACBR1	AR11-	AR13-	AR16-	PACAR2	PACAR2	PACAR2	PACAR2	*PSWAR2	PMBBR2	PMBBR2	PMBBR2	PMBBR2	SW3+	SB06	AR27+	BR27+	M
N	OFLIN-	BR10+	OFTST+	PB03	PB13	PB23	PB33	PSWAR1	PSWAR1	PSWAR1	PSWAR1	PSWBR1	PSWBR1	PSWBR1	PSWBR1	PSWBR1	AR21+	AR23+	AR26+	PSWAR2	PSWAR2	PSWAR2	PSWAR2		PSWBR2	PSWBR2	PSWBR2	PSWBR2	*SW4-	SEL+		CHNRQ+	N
P	G2A01	BR11+	ADO+						*AR14+	*AR15+	*AR16+	*AR17+	*BR14+	*BR15+	*BR16+	*BR17+	AR14+	AR17+	*AR24+	*AR25+	*AR26+	*AR27+			*BR24+	*BR25+	*BR26+	*BR27+	SW4+		CMDCY+	PREND+	P
R		BR12+	CMO+	PB01	PB11	PB21	PB31	IOP4-	BAC08-	BAC09-	BAC10-	BAC11-	BAC08-	BAC09-	BAC10-	BAC11-	GN2A17	AR14-	AR27-	*AR24-	*AR27-			IOP4-	*BR24-	*BR25-	*BR26-	*BR27-	*SW5-		SRVCY+	BRKRQ+	R
S	SELOUT	BR13+	SRO+	PB0	PB1	PB2	PB3	AR1AC-	BAC08-	BAC09-	BAC10-	BAC11-	BAC08-	BAC09-	BAC10-	BAC11-		AR14-	AR17-	BAC08-	BAC09-	BAC10-	BAC11-	AR2AC-	BMB08-	BMB09-	BMB10-	BMB11-	SW5+		CUBSY+	INTRB+	S
T		BR14+	SE0+	PB01	PB11	PB21	PB31	*PACAR1	SW4-	SW5-	SW6-	SW7-	SW4-	SW5-	SW6-	SW7-	GN2A17	AR24-	AR27-	SW4-	SW5-	SW6-	SW7-	*PACAR2	SW4-	SW5-	SW6-	SW7-	*SW6-		CMDLY+	SKIP+	T
U	SELPRP	BR15+	OPO+						SW4+	SW5+	SW6+	SW7+	SW4+	SW5+	SW6+	SW7+				SW4+	SW5+	SW6+	SW7+		SW4+	SW5+	SW6+	SW7+	SW6+		CHSRV+	EACENB	U
V	OLR+	BR16+	SU0+					PACAR1	PACAR1	PACAR1	PACAR1	PACBR1	PACBR1	PACBR1	PACBR1	PACBR1	GN2A17	GN2A17	GN2A17	PACAR2	PACAR2	PACAR2	PACAR2		PMBBR2	PMBBR2	PMBBR2	PMBBR2					V

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
	W028S	W028S	R123	W501	W501	W501	W501	R123	R123	R123	R123	R123	R123	R123	R123	R603	R002	R107	R107	R602	R123	R123	R123	R603	R123	R123	R123	R123	W002	W021CR	W028S	W028S	
A																																	A
B																																	B
C																				GN2B20				GN2B24									C
D	TEST	PB0		SWCTL	ZIPCTL	PWCLR-	SWRST	AR10+	AR11+	AR12+	AR13+	B00-	B06-	BR11+	B02+	SWBR1	BR10-	*EAC00+	*EAC06+		AR20+	AR21+	AR23+	SWBR2	BR20+	BR21+	BR22+	BR23+	B00-	REQ1	BBIP+	BOP+	D
E	SRO0	PB1						AR14+	AR15+	AR16+	AR17+	B01-	B07-	BR15+	B06+	*OFTST-	BR11-	EAC00-	EAC06-	IOP2-	AR24+	AR25+	AR27+	*OFTST-	BR24+	BR25+	BR26+	BR27+	B01-	SEL1-	BBI0+	B00+	E
F	SCMO	PB2	OFTST-	*SWCTL	*ZIPCTL	*PWCLR-	*SWRST	AR1AC-	AR1AC+	AR1AC+	AR1AC+	BOAR1+	BOAR1+	BR1AC+	BOBR1+	PSWBR1	*BR1=0	*EAC01+	*EAC07+	BR1AC-	AR2AC-	AR2BI+	AR2AC-	PSWBR2	SEL1+	SEL1+	SEL1+	SEL1+	B02-		BBI1+	B01+	F
H	SSR0	PB3	*PB4					*EAC04-	*EAC05-	*EAC06-	*EAC07-	*AR10+	*AR16+	*EAC05-	*BR12-		BR12-	EAC01-	EAC07-	BOAR1-	*EAC04-	*BBI1-	*EAC07-		*MB04	*MB05	*MB06	*MB07	B03-		BBI2+	B02+	H
J	SSE02	PB4	*PB5					*EAC08-	*EAC09-	*EAC10-	*EAC11-	*AR11+	*AR17+	*EAC09-	*BR16-		BR13-	EAC02-	EAC08-	GN2B20	*EAC05-	*BBI5-	*EAC08-		*MB08		*MB10	*MB11	B04-		BBI3+	B03+	J
K	SOP0	PB5		PB42	PB52	PB62	PB72	AR10+	AR11+	AR12+	AR13+	B02-	BR10+	B01+	BR13+	IOP4-	*BR1=0	EAC02-	EAC08-	*PDCBR1	AR20+	AR22+	AR23+	BT2A-	BR20+	BR21+	BR22+	BR23+	B05-	INTRPT	BBI4+	B04+	K
L	SSU0	PB6		PB42	PB52	PB62	PB72	AR14+	AR15+	AR16+	AR17+	B03-	BR14+	B05+	BR17+	BR1AC-	BR14-	*EAC03+	*EAC09+	PWCLR-	AR24+	AR26+	AR27+	BRKST-	BR24+	BR25+	BR26+	BR27+	B06-		BBI5+	B05+	L
M	SW0+	PB7	OFTST-	PB43	PB53	PB63	PB73	AR1BI+	AR1BI+	AR1BI+	AR1BI+	BOAR1+	BR1AC+	BOBR1+	BR1AC+	*PACBR1	BR15-	EAC03-	EAC09-		AR2BI+	AR2AC-	AR2BI+	*PMBBR2	BR2BI+	BR2BI+	BR2BI+	BR2BI+	B07-	SKIP	BBI6+	B06+	M
N	SW1+	OLSW1	*PB7					BBI0-	*BBI1-	*BBI2-	*BBI3-	*AR12+	*EAC04-	*BR15-	*EAC11-		BR16-	EAC04-	EAC10-		*BBI4-	*EAC10-	*BBI3-		*BBI0-	*BBI1-	*BBI2-	*BBI3-	B0P-		BBI7+	B07+	N
P	SW2+	OLSW2	*PB7					*BBI4-	*BBI5-	*BBI6-	*BBI7-	*AR13+	*EAC08-	*BR15-	*EAC11-										*BBI4-	*BBI5-	*BBI6-	*BBI7-	BBI0-		CTL00+	CTL06+	P
R	SW3+			PB41	PB51	PB61	PB71	B00+	B01+	B02+	B03+	B04-	B00+	BR12+	B03+	IOP4-	BR17-	*EAC05+	*EAC11+	BRKST-	AR21+	AR22+		SUOP0	B00+	B01+	B02+	B03+	BBI4-		CTL01+	CTL07+	R
S	SW4+	ONLIN+		PB4	PB5	PB6	PB7	B04+	B05+	B06+	B07+	B05-	B04+	BR16+	B07+	CTLAC-	*BR1=0	EAC05-	EAC11-	ZBR2	AR25+	AR26+		GN2B24	B04+	B05+	B06+	B07+	BBI5-		CTL02+	CTL08+	S
T	SW5+	SSE01		PB41	PB51	PB61	PB71	BOAR1+	BOAR1+	BOAR1+	BOAR1+	BOAR1+	BOBR1+	BR1AC+	BOBR1+	*PBAC		TSTIO-	*SW7-	GN2B20	AR2AC-	AR2BI+	PWCLR-	*SYSRST	BOBR2+	BOBR2+	BOBR2+	BOBR2+	BBI6-		CTL03+	CTL09+	T
U	SW6+	*						*AR10-	*AR11-	*AR12-	*AR13-	*AR14+	*BR10-	*EAC06-	*BR13-					*PDCBR2	*EAC05-	*BBI2-	*CMDCY+		*BR20-	*BR21-	*BR22-	*BR23-	BBI7-		CTL04+	CTL10+	U
V	SW7+	*						*AR14-	*AR15-	*AR16-	*AR17-	*BR15+	*BR14-	*EAC10-	*BR17-		BR1=0	*		PWCLR-	*EAC09-	*BBI6-	*SRVCY+	SWRST	*BR24-	*BR25-	*BR26-	*BR27-	BBIP-		CTL05+	CTL11+	V

PANEL 3 ... CONTROL REGISTER AND SEQUENCE GATING

Table A (A01–A32)

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
type	W021CR	W021CR	W021CR	W021CR	R123	R113	R205	R121	R121	R121	R121	R121	R107	R107	R121	R121	R121	R121	R107	R121	R121	R151	R113	R107	R123	R141	R107	W021CR	W021CR	W021CR	W021CR	W021CR
C	GN3A01						GN3A07															GN3A22			GN3A26							GN3A28
D	AC00	AC00	MB00	MB00	EAC00+	B0REQ-		≪CHSRS	≪BADI+	≪PREND-	≪CTL10-	≪TSTIO+	≪AR1BI+	≪CMINT-	≪INTR8+	≪SROBUR	≪REQ1	≪RSTCMD	≪BT2A-	≪SRINT+	≪CHNRQ+	GN3A22	BOR1	≪BOREQ-	CTL00+	≪ACTEST	≪BAC00+	EAC00-	BAC00-	BAC00-	BMB00-	BMB00-
E	AC01	AC01	MB01	MB01	EAC01+	SEL1+	≪CMDLY-	CMDLY+	AR1BI+	PREND+	ADO+	TSTIO-	AR1BI-	CMINT+	CMINT-	BURST+	SROBUR	CHINT-	BT2A	CTL10-	SRVCY+	CTL01-	BOR2	BOREQ+	CTL01+	BAC00+	BAC00-	EAC01-	BAC01-	BAC01-	BMB01-	BMB01-
F	GN3A01	GN3A01	GN3A01	GN3A01	EACAC+	≪XFER	BOPI+	CMO-	AR2BI-	ZCTLO	SRVCY-		≪AR2BI+	≪SPSTA+	SRINT-	SRO÷	BRKRQ+	SCCC	≪BT1-	CTL11-	SRO+	CTL01+	≪BOREQ+	≪	CTLAC+	EAC00-	≪BAC01+	GN3A28	GN3A28	GN3A28	GN3A28	GN3A28
H	AC02	AC02	MB02	MB02	≪AC00	EACENB	GN3A07	≪CHSRV+	≪AR2BI-	≪CTL11-	≪CTL10-	≪CTL07-	AR2BI-	SPSTA-	≪40BI-	≪10BI-	≪DC6	≪SCCC	BT1	≪BURBRK	CLRCR+	CTL00+	BIR1		≪EAC00-	BAC01+	BAC01-	EAC02-	BAC02-	BAC02-	BMB02-	BMB02-
J	GN3A01	GN3A01	GN3A01	GN3A01	≪AC01	IOP1	≪CMDLY+	RSTCHN	CMDLY-	PREND-	SRVCY+	CMO+	≪BOBR1+	00BI+	SPSTA+	SRO+	PWCLR-	SRO+	≪IOP4-	BURST-	PWCLR-	CTL00-	CTL02-	≪BIREQ+	BURST+	BAC02+	BAC02-	EAC03-	BAC03-	BAC03-	BMB03+	BMB03+
K	AC03	AC03	MB03	MB03	EAC02+	≪EACAC-			SRVCY+	CTL10+	OPO-	00BI+	B0BR1-	CMSTA-	TSTIO+	TSTIO-	ZIPCTL	CMDCY+	IOP4	BRKRQ+	CTL10-	CTL02-	≪BIREQ+	BURST+	CTL02+	BAC02+	BAC02-	EAC03-	BAC03-	BAC03-	BMB03+	BMB03+
L	GN3A01	GN3A01	GN3A01	GN3A01	EAC03+	RDENB+		≪B0BR1-	≪AR1BI-	≪CTL11-	≪CTL10-	≪CTL09-	≪ADDAC-	≪CHNRQ+	≪CMSTA-	≪SPSTA-	≪DC3	≪SCCC	≪IOP2-	≪SYCVCO	≪BMB30	CTL02+	STR1	≪AR1AC-	CTL03+	EAC02-	≪BAC03+	GN3A28	GN3A28	GN3A28	GN3A28	GN3A28
M	AC04	AC04	MB04	MB04	EACAC+	IOP1	CDY3	BADI+	CMDCY+	PREND+	SRVCY+	00BI+	ADDACP	CLRCR+	CMDCY+	CMDCY+	SYSRST	CMDCY+	IOP2	SRVCY+	BMB03-	≪		STR2	AR1AC-	CTLAC-	BAC03+	EAC04-	BAC04-	BAC04-	BMB03-	BMB03-
N	GN3A01	GN3A01	GN3A01	GN3A01	≪AC02	CHSRS	CMO+	ADO-	SRO+	SRVCY-	CMO+	TSTIO-	PREND-	SEL1+	CHSRV+	SRVCY+	ZIPCTL	CMO+	SRINT+	CMO+	BMB05+	≪BQR1	STR2	BR1AC-	≪EAC03-	BAC04+	BAC04-	EAC05-	BAC05-	BAC05-	BMB04+	BMB04+
P	AC05	AC05	MB05	MB05	≪AC03	BURST+	≪CHSRV-	≪SBMA	≪BRKRQ-	≪CTL11-	≪PREND-	≪CTL08-	≪RDENB+	≪SEL1+	≪SRSTA-	≪BSTI+	≪DC0	≪SCCC	≪CTL0Z+	≪CMINT+	≪SBM	≪BQR2	SU0+	≪AR2AC+	CTL04+	EAC04-	≪BAC05+	GN3A28	GN3A28	GN3A28	GN3A28	GN3A28
R	GN3A01	GN3A01	GN3A01	GN3A01	EAC04+	BRKRQ+	≪CHSRV-	≪SBMA	≪BRKRQ-	≪CTL11-	≪PREND-	≪CTL08-	≪RDENB+	≪SEL1+	≪SRSTA-	≪BSTI+	≪DC0	≪SCCC	≪CTL0Z+	≪CMINT+	≪SBM	≪BQR2	SU0+	≪AR2AC+	CTL04+	EAC04-	≪BAC05+	GN3A28	GN3A28	GN3A28	GN3A28	GN3A28
S	AC06	AC06	MB06	MB06	EAC05+	≪BURBK-	SBMA	SRINT-	SRO÷	BTBRK+		CMDCY+	RDENB	SEL1-	CMDCY-	CMSTA-	SYSRST	CMDCY+	SRINT-	CTL06-	SRINT-	≪BIR1	≪DISABL	AR2AC-	CTL05-	EAC05-	≪BAC06+	EAC06-	BAC06-	BAC06-	BMB04-	BMB04-
T	AC07	AC07	MB07	MB07	EACAC+	BURBK-	GN3A07	BRKSTA	PREND-	BOREQ+	SEL1+	ADO+	≪EACAC+	≪BOPI+	SRVCY+	SRSTA-	PWCLR-	OPO-	≪CTL0Z-	CTL07-	BRKSTA	≪BIR2	BOR2	≪CTLAC-	CTL05+	EAC05-	≪BAC06+	EAC07-	BAC07-	BAC07-	BMB05+	BMB05+
U	GN3A01	GN3A01	GN3A01	GN3A01	≪AC04	BOPI+		SEL1+	SRVCY+	SEL1+	WC=0	SEO-	EACAC-	BOPI+	CHSRV+	SPSTA-	CTL0Z+	SU0+	CTL0Z+	CTL08-	SEL1+	≪STR1	BIR2	CTLAC-	CTL04+	≪EAC04-	GN3A26	BAC06-	GN3A28	GN3A28	GN3A28	GN3A28
V	AC08	AC08	MB08	MB08	≪AC05	≪RSTCHN	BT2A-	SRVCY+	SRINT-	PREND+						STREQ+	CUBSY-	ZIPCTL		CTL09-	SRVCY-	≪STR2		≪BURST+			≪EAC05-				BMB05-	BMB05-

Table B (B01–B32)

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
type	W021CR	W021CR	W021CR	W021CR	R123	R121	R001	R111	R121	R107	R121	R121	R107	R111	R001	R205	R205	R205	R205	R205	R205	R205	R151	W002	R123	R141	R107	W021CR	W021CR	W021CR	W021CR	W021CR
C	GN3B01															GN3B17	GN3B18									GN3B26						GN3B28
D	AC09	AC09	MB09	MB09	EAC06+	≪BOPI+	BOPAR-	OPO+	≪PROP3	≪OURAD+	≪OURCM1	≪OURCM4	≪CUBSY+	CMDCY+	CHNRQ+	PBAC	PBAC	PBAC	PBAC	PBAC	PBAC	BMB30	EAC00-	CTL06+	≪ACTEST	≪BAC07+	EAC09-	BAC09-	BAC09-	BAC09-	BMB06+	BMB06+
E	AC10	AC10	MB10	MB10	EAC07+	CMDCY-	≪EXTADD	ADO+	PROP1	OURAD-	CMINT-	OURCM3	CUBSY-	AR=AR	≪CSAC	≪CTL00-	≪CTL02-	≪CTL06-	≪CTL03-	≪CTL05-	≪CTL08-	≪CTL10-	BMB07+	EAC01-	CTL07+	BAC06-	BAC07-	EAC10-	BAC10-	BAC10-	BMB06-	BMB06-
F	GN3B01	GN3B01	GN3B01	GN3B01	EACAC+	SRVCY-	≪EXTADD	ADRDT+	EXTADD	PROP2	SEL+	OURAD+	SEL+	CSAC	CSAC	PWCLR-	SYSRST	ZCTL3	ZCTL3	ZCTL3	ZCTL3	GN3B18						BAC07+	BAC08-	GN3B28	BMB07+	BMB07+
H	AC11	AC11	MB11	MB11	≪AC06	≪CTLSKP	≪EXTADD	OURAD-	PROP2	SEL-	OURCM2	SEL+	≪SRVCY-	BOAR1-	SRVCY-	≪CSAC	SW0-	SW2-	GN3B18				BMB06+	EAC03-	≪EAC06-	BAC07+	BAC08-	EAC11-	BAC11-	BAC11-	BMB07+	BMB07+
J	GN3B01	GN3B01	GN3B01	GN3B01	≪AC07	SKPENB	BOPI-	OURAD-	PROP3	≪PWCLR+	OURCM1	SEL+	≪CMDCY+	AR=AR	BADI+	≪CTL00+	≪CTL02+	≪CTL06-	≪CTL03+	≪CTL05+	≪CTL08+	≪CTL10+	BMB06-	EAC04-	≪EAC07-	BAC07+	≪BAC09+	EAC07-	BAC08-	GN3B28	GN3B28	GN3B28
K	SKIP	SKIP	CYCSEL	CYCSEL	EAC08+	CTLAC-	≪EXTADD	OPO+	SEO+	PWCLR	CUBSY-	SRVENB	RSTCMD	INTR8+	≪CSAC	BAC00-	BAC02-	BAC06-	BAC03-	BAC05-	BAC08-	BAC10-	BMB08-	EAC05-	CTL08+	BAC08+	BAC09-	RDENB	IOP1	IOP1	BMB07-	BMB07-
L	GN3B01	GN3B01	GN3B01	GN3B01	EAC09+	≪PROP1	DISABL	ADO-	≪SEL-	≪CUBSY-	≪CMDCY+	≪CMDCY+	CMO-	BAC00-	BAC02-	BAC06-	BAC03-	BAC05-	BAC08-	BAC10-			≪AR1AC-	EAC07-	CTLAC-	BAC09-	BAC10-	SKPENB	IOP2	IOP2	BMB08+	BMB08+
M	INTRPT	INTRPT	MBJ1	MBJ1	EACAC+	BREI-	≪EXTREQ	EXTREQ	PROP1	OURCM2	BOAR1-	CMDCY+	≪SRVCY+	≪INTRPT	SYCVCO	PBAC	ADDAC-	BOREQ-	PBAC	PBAC	PBAC	PBAC	≪BR1AC-	EAC08-	≪EAC08-	EAC09-	≪BAC11+	GN3B28	GN3B28	GN3B28	BMB08-	BMB08-
N	GN3B01	GN3B01	GN3B01	GN3B01	≪AC08	OURAD-	CHNRQ+	≪BREI-	SEO+	≪ZCTLO	SEL+	CMDCY-	≪SRVCY+	≪INTRPT	SYCVCO	PBAC	ADDAC-	BOREQ-	PBAC	PBAC	PBAC	PBAC	≪BR1AC-	EAC08-	≪EAC08-	EAC09-	≪BAC11+	GN3B28	GN3B28	GN3B28	BMB08-	BMB08-
P	ACCLR	ACCLR	WC=0	WC=0	≪AC09	SEL-	≪EXTREQ	BREI-	PROP2	DCO	OURCM4	SRVCY-	CMO-	≪SYCVC1	≪CTL01+	≪BRKRQ+	≪CHNRQ+	≪CTL04+	≪CTL07+	≪CTL09+	≪CTL11+	≪AR2AC-	EAC09-	≪EAC09-	BAC10+	BAC11-			IOP4	IOP4	BMB08-	BMB08-
R	GN3B01	GN3B01	GN3B01	GN3B01	EAC10+	≪EACENB	BOPI-	IOP2	≪SPROP-	≪ZCTL3	≪OURCM3	≪BOAR1-	≪SRVCY-	SRINT-	≪SYCVC0	≪CTL01-	≪BRKRQ-	GN3B17	≪CTL04-	≪CTL07-	≪CTL09-	≪CTLAC-	EAC10-	CTL10-	≪IOP2-	GN3B28			BT1	BT1	BMB09-	BMB09-
S	RUN	RUN	MBJ2	MBJ2	EAC11+	BR1AC-	BOPI-	IOP2	PROP3	ZCTL6	OURCM2	CUBSY-	SRVCY-	BURBRK	≪CTL02+	BAC01-	SBM	BAC04-	BAC07-	BAC09-	BAC11-	≪		EAC11-	CTL11-	BAC11-	≪IOP2-	GN3B28			BMB09-	BMB09-
T	ACJ1	ACJ1	MBJ3	MBJ3	EACAC+	BR1AC-	CTLSKP	CTLSK1	PROP3	≪ZCTL6	OURCM4	QURAD+	≪SRVCY+	SYCVC1	ZCTL0	BAC01-		BAC04-	BAC07-	BAC09-	BAC11-	≪		ACTEST	CTLAC+	EAC11-	≪IOP4-	BT2A	BT2A		BMB10-	BMB10-
U	GN3B01	GN3B01	GN3B01	GN3B01	≪AC10	AR2AC-	≪CTLSK1	≪SKIP	SEL-	DC6	OURCM3	RSTSRV	≪RSTSRV	≪CTL02+	BAC01-	SEL1-		BAC04-	BAC07-	BAC09-	BAC11-	≪		RDENB	≪EAC10-	GN3B26	IOP4	GN3B28	GN3B28	GN3B28	GN3B28	
V	ACJ2	ACJ2	MBJ4	MBJ4	≪AC11	CTLAC-		SEL1-	BOPI-		SEL+		RSTSRV	≪CTL02+		SWCTL	CTL00-	BT2A-							SKPENB	≪EAC11-					PWRCLR	PWRCLR	BMB11-

APPENDIX F

MAINTENANCE AND DIAGNOSTIC FACILITIES

MAINTENANCE AND DIAGNOSTIC FACILITIES

F1. The Test Panel

The System/360 interface contains facilities for
self-checking during its operation and for diagnosing circuit
faults. Maintenance operations can be carried out both on-
and off-line using built-in test controls and indicators.
Precipitous fault conditions can be detected with conventional
perturbation methods using the margin-check power supply of
the PDP-8. The principal test component is the Test Panel,
shown in Figure F1. The top two rows of indicators on the
left on this panel monitor the contents of the four principal
data registers of the interface: AR1, AR2, BR1, and BR2.
The next two rows of indicators monitor the status of the
channel interface tag lines and bus lines. The upper row
of these monitors information placed by the interface on the
inbound lines to the channel; the lower row monitors informa-
tion placed by the channel on the outbound lines to the inter-
face. Beneath these indicators is a row of switches used to
simulate the outbound lines in off-line operation. The large
pushbutton at the extreme lower right controls the on/off-
line status of the interface. None of the test controls are
operable when this switch in the on-line position, although
the various indicators continue to monitor the state of the
circuitry. When the equipment is in the off-line or test
condition the signals to the channel lines are deactivated
in such a way that servicing operations and power up/down
sequencing can be conducted without in any way affecting the
operations by the channel with other control units. To the
right of the block of indicators just described is a block
of 24 indicators which monitor the status of most of the
control flip-flops of the interface. These can be roughly
grouped as follows: If one of the top row of indicators is
lit, then the interface is actively communicating with the

ADR REG 1   ADR REG 2

BUF REG 1   BUF REG 2

CU SEL   CMD CYC   CMD CYC   SRV CYC   CU BZY   CMD DLY   CHL SRV

CHL REQ   PRP END   BRK REQ   INT REQ   SKP REQ   EAC

CTL OP   0   1   2

CMD CHN   CMD PCK   SRV PCK

GOD ADR STA   TAGS IN   SRV   SEL   OPL REQ

SYS RST   CMD STK   CMD HLT   CMD END   CMD HLT   SRV END

TST ADR CMD   TAGS OUT   SRV   SEL   OPL SUP

BUSS IN   P   0   1   2   3   4   5   6   7

BUSS OUT   P   0   1   2   3   4   5   6   7

TST ADR CMD   TAGS OUT   SRV   SEL   OPL SUP

BUSS OUT   P   0   1   2   3   4   5   6   7

REG LOAD   AR1   BR1   AR2   BR2   CTL OP   CTL CLR   PWR CLR   SYS RST

REG DATA   0   1   2   3   4   5   6   7

ON LINE

FIGURE F1.   TEST PANEL LAYOUT.

channel. During various parts of a channel-interface opera-
tion, the next row of indicators may be lit. A service
cycle (data or status) will result in alternate operation
of the CHL REQ and BRK REQ indicators. The last two rows
of indicators represent the contents of the CTL register
exactly as indicated to the resident PDP-8 program.

F2. Diagnostic Procedures

In normal system operations the interface is on-
line to the System/360 as indicated by the illuminated push-
button switch at the lower right of the test panel. Alter-
nate depressions of this pushbutton switch the interface
from the on-line, to the off-line state and vice versa. In
the off-line state the interface is logically disconnected
from the System/360 channel-control unit lines and may be
tested independently of the System/360 using the manual
controls on the test panel and certain PDP-8 test programs
constructed for this purpose and described below.

In some situations it is desirable to activate
the manual controls on the test panel when the interface
is on-line to the System/360. A special override switch
(TEST) is provided for this purpose. The lamp above this
switch indicates, when lit, that the manual controls are
operative.

The interface contains special circuitry which
prevents transitions to and from the on-line state when
channel operations are pending at the interface. There-
fore servicing operations involving such transitions can
proceed without disturbing the System/360. Following is a
description of diagnostic utilities intended to ferret out
most component failures.

360 INTERFACE REGISTER TEST

Purpose

Program tests AR1, BR1, AR2, and CTL gating with the AC, and in addition tests BR2 gating with the MB. Read, Clear, and Write operations are tested with AR1, BR1, and AR2. Read, test-under-mask and invert under-mask operations are tested with CTL. The interrupt facility is tested in conjunction with CTL; and the 3-cycle data break facility is tested in conjunction with BR2.

DIRECTIONS FOR USE

a. Switch interface off-line.
b. START program at 200. Program will stop at 214.
c. Using manual controls, load all ones (377 octal) into AR1, BR1, and AR2. Press CONTINUE.
d. Program will loop through all tests in about 3 seconds Error stops are documented in program listing.

360 INTERFACE ECHO TEST

Purpose

Program tests all channel interface circuitry except bus drivers, receivers and on-line/off-line circuitry. Channel interface sequences are simulated with the manual controls.

DIRECTIONS FOR USE

a. Switch interface off-line. Raise OPL OUT and BUS OUT (P) switches.
b. Load program. START at 0200. Lower SR switches. Program will loop.
c. System Reset. Lower OPL OUT switch. Program will stop at 221. AC will contain 0040 and SYS RST lamp will be on in CTL. Raise OPL OUT; press CONTINUE.

```
/SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES              PAGE   1
/
/*****************************************************************
/*                                                             *
/*        SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES             *
/*                                                             *
/*****************************************************************
/
/INTERFACE REGISTER DEFINITIONS
/
RD=1                      /IOP READ
CLR=2                     /IOP CLEAR
TST=2                     /IOP TEST
WR=4                      /IOP WRITE
INV=4                     /IOP INVERT
AR1=6300                  /ADDRESS REGISTER 1
BR1=6310                  /BUFFER REGISTER 1
AR2=6320                  /ADDRESS REGISTER 2
CTL=6330                  /CONTROL REGISTER
/
/INTERFACE CONTROL REGISTER BIT DEFINITIONS
/
STREQ=7000                /STATUS REQUEST
BIREQ=4000                /BUS-INBOUND SERVICE REQUEST
BOREQ=2000                /BUS-OUTBOUND SERVICE REQUEST
CMDCHN=0400               /COMMAND CHAIN
CMDPCK=0200               /BUS-OUT PARITY CHECK ON COMMAND BYT
SRVPCK=0100               /BUS-OUT PARITY CHECK ON DATA BYTE
CMDRST=0040               /SYSTEM OR SELECTIVE RESET
CMDSTK=0020               /STACK STATUS ON INITIAL SELECTION
CMDHLT=0010               /HALT I/O
CMDEND=0004               /COMMAND ACCEPT
SRVHLT=0002               /SERVICE STOP
SRVEND=0001               /PDP-8 WC=0
/
/SYSTEM/360 STATUS BYTE DEFINITIONS
/
UNCHCK=002                /02 UNIT CHECK
DEVEND=004                /04 DEVICE END
CHNEND=010                /08 CHANNEL END
/
*1
/
0001  5420           JMP I INTRPT
            BR2BLK,*.+2
/
*10
            AXR1,  *.+1
/
*20
0020  0100   INTRPT,INTX
0021  0001   BR2DBP,BR2BLK-1
0022  0035   BR2CA, TMP3-1
0023  0002   XSRHLT,SRVHLT
0024  2000   XBOREQ,BOREQ
0025  4000   XBIREQ,BIREQ
0026  0377   K0377, 0377
0027  0777   K0777, 0777
0030  7000   K7000, 7000
0031  7400   K7400, 7400
```

/SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES   PAGE   2

```
                   /
0032    7767    K7767,  7767
0033    7772    K7772,  7772
                   TMP1,   *.+1
                   TMP2,   *.+1
                   TMP3,   *.+1
                   AC,     *.+1
                   /
                   *100
                   /
                   /
                   /INTERRUPT ROUTINE
                   /
0100    3037    INTX,   DCA AC
0101    6042            TCF
0102    6032            KCC
0103    6331            CTL RD
0104    0027            AND K0777
0105    7640            SZA CLA
0106    2000            ISZ 0
0107    1037            TAD AC
0110    5400            JMP I 0
                   /
                   /START USING START KEY
                   /
                   *200
                   /
                   /TEST AR1, BR1, AR2 REGISTERS
                   /
0200    6301    START,  AR1 RD
0201    7440            SZA
0202    7402            HLT             /AR1-AC GATES PICKED UP A BIT (AC)
0203    7200            CLA
0204    6311            BR1 RD
0205    7440            SZA
0206    7402            HLT             /BR1-AC GATES PICKED UP A BIT (AC)
0207    7200            CLA
0210    6321            AR2 RD
0211    7440            SZA
0212    7402            HLT             /BR2-AC GATES FAILED A BIT (AC)
0213    7200            CLA
0214    7402            HLT             /OPERATOR ACTION PAUSE
                   /
                   /LOAD ONES INTO AR1, BR1, AND BR2 USING MANUAL
                   /CONTROLS. RESTART USING CONTINUE KEY
                   /
0215    1031    AR1T1,  TAD K7400
0216    6301            AR1 RD
0217    7040            CMA
0220    7440            SZA
0221    7402            HLT             /AR1-AC GATES DROPPED A BIT (AC)
0222    7200            CLA
0223    6302            AR1 CLR
0224    6301            AR1 RD
0225    7440            SZA
0226    7402            HLT             /CLEAR AR1 GATES FAILED A BIT (AC)
0227    7240            STA
0230    6304            AR1 WR
0231    0031            AND K7400
```

/SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES   PAGE   3

```
                    /
0232  6301          AR1 RD
0233  7040          CMA
0234  7440          SZA
0235  7402          HLT              /AC-AR1 GATES DROPPED A BIT (AC)
0236  7200          CLA
0237  6304          AR1 WR
0240  1031          TAD K7400
0241  6301          AR1 RD
0242  7040          CMA
0243  7440          SZA
0244  7402          HLT              /AC-AR1 GATES INVERTED A BIT (AC)
0245  7200          CLA
                    /
0246  1031  BR1T1,  TAD K7400
0247  6311          BR1 RD
0250  7040          CMA
0251  7440          SZA
0252  7402          HLT              /BR1-AC GATES DROPPED A BIT (AC)
0253  7200          CLA
0254  6312          BR1 CLR
0255  6311          BR1 RD
0256  7440          SZA
0257  7402          HLT              /CLEAR BR1 GATES FAILED A BIT (AC)
0260  7240          STA
0261  6314          BR1 WR
0262  0031          AND K7400
0263  6311          BR1 RD
0264  7040          CMA
0265  7440          SZA
0266  7402          HLT              /AC-BR1 GATES DROPPED A BIT (AC)
0267  7200          CLA
0270  6314          BR1 WR
0271  1031          TAD K7400
0272  6311          BR1 RD
0273  7040          CMA
0274  7440          SZA
0275  7402          HLT              /AC-BR1 GATES INVERTED A BIT (AC)
0276  7200          CLA
                    /
0277  1031  AR2T1,  TAD K7400
0300  6321          AR2 RD
0301  7040          CMA
0302  7440          SZA
0303  7402          HLT              /AR2-AC GATES DROPPED A BIT (AC)
0304  7200          CLA
0305  6322          AR2 CLR
0306  6321          AR2 RD
0307  7440          SZA
0310  7402          HLT              /CLEAR AR2 GATES FAILED A BIT (AC)
0311  7240          STA
0312  6324          AR2 WR
0313  0031          AND K7400
0314  6321          AR2 RD
0315  7040          CMA
0316  7440          SZA
0317  7402          HLT              /AC-AR2 GATES DROPPED A BIT (AC)
0320  7200          CLA
0321  6324          AR2 WR
```

```
                  /SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES          PAGE  4
                  /
0322  1031              TAD K7400
0323  6321              AR2 RD
0324  7040              CMA
0325  7440              SZA
0326  7402              HLT                    /AC-AR2 GATES INVERTED A BIT (AC)
0327  7200              CLA
                  /
0330  5731              JMP I .+1
0331  0400              AR1T2
                  /
                  *400
                  /
                  /TEST AR1, BR1, AR2 REGISTERS
                  /
0400  3034  AR1T2,  DCA TMP1
0401  1034          TAD TMP1
0402  6306          AR1 CLR+WR
0403  0031          AND K7400
0404  6301          AR1 RD
0405  3035          DCA TMP2
0406  1035          TAD TMP2
0407  7040          CMA
0410  0034          AND TMP1
0411  7440          SZA
0412  7402          HLT                    /AR1 ECHO DROPPED A BIT (AC)
0413  7200          CLA
0414  1034          TAD TMP1
0415  7040          CMA
0416  0035          AND TMP2
0417  7440          SZA
0420  7402          HLT                    /AR1 ECHO PICKED UP A BIT (AC)
0421  7200          CLA
0422  2034          ISZ TMP1
0423  5201          JMP AR1T2+1
                  /
0424  3034  BR1T2,  DCA TMP1
0425  1034          TAD TMP1
0426  6316          BR1 CLR+WR
0427  0031          AND K7400
0430  6311          BR1 RD
0431  3035          DCA TMP2
0432  1035          TAD TMP2
0433  7040          CMA
0434  0034          AND TMP1
0435  7440          SZA
0436  7402          HLT                    /BR1 ECHO DROPPED A BIT (AC)
0437  7200          CLA
0440  1034          TAD TMP1
0441  7040          CMA
0442  0035          AND TMP2
0443  7440          SZA
0444  7402          HLT                    /BR1 ECHO PICKED UP A BIT (AC)
0445  7200          CLA
0446  2034          ISZ TMP1
0447  5225          JMP BR1T2+1
                  /
0450  3034  AR2T2,  DCA TMP1
0451  1034          TAD TMP1
```

/SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES   PAGE   5

```
                 /
0452  6326       AR2 CLR+WR
0453  0031       AND K7400
0454  6321       AR2 RD
0455  3035       DCA TMP2
0456  1035       TAD TMP2
0457  7040       CMA
0460  0034       AND TMP1
0461  7440       SZA
0462  7402       HLT              /AR2 ECHO DROPPED A BIT (AC)
0463  7200       CLA
0464  1034       TAD TMP1
0465  7040       CMA
0466  0035       AND TMP2
0467  7440       SZA
0470  7402       HLT              /AR2 ECHO PICKED UP A BIT (AC)
0471  7200       CLA
0472  2034       ISZ TMP1
0473  5251       JMP AR2T2+1
                 /
0474  5675       JMP I .+1
0475  0600       CTLT1
                 /
                 *600
                 /
                 /TEST CONTROL REGISTER GATING
                 /
0600  6331  CTLT1, CTL RD
0601  7440       SZA
0602  7402       HLT              /CTL-AC GATES PICKED UP A BIT (AC)
0603  7200       CLA
0604  1027       TAD K0777
0605  6334       CTL INV
0606  7200       CLA
0607  1030       TAD K7000
0610  6331       CTL RD
0611  7040       CMA
0612  7440       SZA
0613  7402       HLT              /CTL-AC GATES DROPPED A BIT (AC)
0614  7200       CLA
0615  1027       TAD K0777
0616  6334       CTL INV
0617  7200       CLA
0620  6331       CTL RD
0621  7440       SZA
0622  7402       HLT              /CTL FAILED TO INVERT A BIT (AC)
0623  7200       CLA
                 /
0624  3034  CTLT2, DCA TMP1
0625  1034       TAD TMP1
0626  6334       CTL INV
0627  7200       CLA
0630  6331       CTL RD
0631  3035       DCA TMP2
0632  1035       TAD TMP2
0633  7040       CMA
0634  0034       AND TMP1
0635  7440       SZA
0636  7402       HLT              /CTL ECHO DROPPED A BIT (AC)
```

```
                   /
0637    7200            CLA
0640    1034            TAD  TMP1
0641    7040            CMA
0642    0035            AND  TMP2
0643    7440            SZA
0644    7402            HLT                    /CTL ECHO PICKED UP A BIT (AC)
0645    7200            CLA
0646    1034            TAD  TMP1
0647    6334            CTL  INV
0650    7200            CLA
0651    6331            CTL  RD
0652    7440            SZA
0653    7402            HLT                    /CTL FAILED TO INVERT A BIT (AC)
0654    7200            CLA
0655    1034            TAD  TMP1
0656    7001            IAC
0657    0027            AND  K0777
0660    7440            SZA
0661    5224            JMP  CTLT2
                   /
0662    1032    CTLT3,  TAD  K7767
0663    3034            DCA  TMP1
0664    7120            STL
0665    6334    CTLT3A, CTL  INV
0666    6332            CTL  TST
0667    7402            HLT                    /CTL TST FAILED TO SKIP
0670    7040            CMA
0671    6332            CTL  TST
0672    7410            SKP
0673    7402            HLT                    /CTL TST SKIPPED IN ERROR
0674    7040            CMA
0675    6334            CTL  INV
0676    7004            RAL
0677    2034            ISZ  TMP1
0700    5265            JMP  CTLT3A
0701    7200            CLA
                   /
0702    3034    CTLT4,  DCA  TMP1
0703    1034            TAD  TMP1
0704    6334            CTL  INV
0705    7200            CLA
0706    3035    CTL4C,  DCA  TMP2
0707    1035            TAD  TMP2
0710    0034            AND  TMP1
0711    7041            CIA
0712    1035            TAD  TMP2
0713    7640            SZA  CLA
0714    5321            JMP  CTL4A
0715    1035            TAD  TMP2
0716    6332            CTL  TST
0717    7402            HLT                    /CTL TST FAILED TO SKIP
0720    5325            JMP  CTL4B
                   /
0721    1035    CTL4A,  TAD  TMP2
0722    6332            CTL  TST
0723    7410            SKP
0724    7402            HLT                    /CTL TST SKIPPED IN ERROR
0725    7001    CTL4B,  IAC
```

/SYSTEM/360 INTERFACE DIAGNOSTIC ROUTINES   PAGE   7

```
                 /
0726   7440          SZA
0727   5306          JMP CTL4C
0730   6335          CTL RD+INV
0731   7104          CLL RAL
0732   0027          AND K0777
0733   7440          SZA
0734   5302          JMP CTLT4
                 /
0735   1033   CTLT5, TAD K7772
0736   3035          DCA TMP2
0737   7120          STL
0740   7004   CTLT5A,RAL
0741   6334          CTL INV
0742   6001          ION
0743   7000          NOP
0744   7402          HLT              /CTL FAILED TO INTERRUPT
0745   6334          CTL INV
0746   6001          ION
0747   7000          NOP
0750   7410          SKP
0751   7402          HLT              /CTL INTERRUPTED IN ERROR
0752   6002          IOF
0753   2035          ISZ TMP2
0754   5340          JMP CTLT5A
0755   7200          CLA
                 /
0756   5757          JMP I .+1
0757   1000          BR2T1
                 /
                 *1000
                 /
                 /TEST BR2 AND DATA BREAK
                 /
1000   3034   BR2T1, DCA TMP1
1001   1034          TAD TMP1
1002   3036          DCA TMP3
1003   1021          TAD BR2DBP
1004   3010          DCA AXR1
1005   7240          STA
1006   3410          DCA I AXR1
1007   1022          TAD BR2CA
1010   3410          DCA I AXR1
1011   1025          TAD XBIREQ
1012   6334          CTL INV
1013   7200          CLA
1014   3035          DCA TMP2
1015   1021   BR2T1E,TAD BR2DBP
1016   3010          DCA AXR1
1017   1410          TAD I AXR1
1020   7650          SNA CLA
1021   5225          JMP BR2T1A
1022   2035          ISZ TMP2
1023   5215          JMP BR2T1E
1024   7402          HLT              /DB WORD COUNT FAILED TO DECREMENT
1025   1022   BR2T1A,TAD BR2CA
1026   7040          CMA
1027   1410          TAD I AXR1
1030   7440          SZA
```

```
                    /
1031   7402         HLT                  /DB CURRENT ADDRESS FAILED TO INCREM
1032   7200         CLA
1033   1034         TAD TMP1
1034   7041         CIA
1035   1036         TAD TMP3
1036   7440         SZA
1037   7402         HLT                  /DB TRANSFER DIRECTION SENSE WRONG
1040   7200         CLA
1041   1023         TAD XSRHLT
1042   6335         CTL RD+INV
1043   7200         CLA
1044   6335         CTL RD+INV
1045   7200         CLA
1046   3036         DCA TMP3
1047   1021         TAD BR2DBP
1050   3010         DCA AXR1
1051   7240         STA
1052   3410         DCA I AXR1
1053   1022         TAD BR2CA
1054   3410         DCA I AXR1
1055   1024         TAD XBOREQ           /(RATHER UNORTHODOX SEQUENCE)
1056   6334         CTL INV
1057   1025         TAD XBIREQ
1060   6334         CTL INV
1061   6334         CTL INV
1062   7200         CLA
1063   3035         DCA TMP2
1064   1021  BR2T1D,TAD BR2DBP
1065   3010         DCA AXR1
1066   1410         TAD I AXR1
1067   7650         SNA CLA
1070   5274         JMP BR2T1C
1071   2035         ISZ TMP2
1072   5264         JMP BR2T1D
1073   7402         HLT                  /DB WORD COUNT FAILED TO DECREMENT
1074   1022  BR2T1C,TAD BR2CA
1075   7040         CMA
1076   1410         TAD I AXR1
1077   7440         SZA
1100   7402         HLT                  /DB CURRENT ADDRESS FAILED TO INCREM
1101   7200         CLA
1102   1023         TAD XSRHLT
1103   6335         CTL RD+INV
1104   7200         CLA
1105   6335         CTL RD+INV
1106   7200         CLA
1107   1036         TAD TMP3
1110   0031         AND K7400
1111   7440         SZA
1112   7402         HLT                  /DB PICKED UP BITS IN POS 0-3
1113   7200         CLA
1114   1034         TAD TMP1
1115   0031         AND K7400
1116   1036         TAD TMP3
1117   3036         DCA TMP3
1120   1034         TAD TMP1
1121   7040         CMA
1122   0036         AND TMP3
```

```
                    /
1123   7440         SZA
1124   7402         HLT                    /BR2 ECHO FAILED
1125   7200         CLA
1126   1036         TAD TMP3
1127   7040         CMA
1130   0034         AND TMP1
1131   7440         SZA
1132   7402         HLT                    /BR2 ECHO FAILED
1133   7200         CLA
1134   2034         ISZ TMP1
1135   5201         JMP BR2T1+1
                    /
1136   5737         JMP I .+1
1137   0215         AR1T1
                    /
AC        0037
AR1       6300
AR1T1     0215
AR1T2     0400
AR2       6320
AR2T1     0277
AR2T2     0450
AXR1      0010
BIREQ     4000
BOREQ     2000
BR1       6310
BR1T1     0246
BR1T2     0424
BR2BLK    0002
BR2CA     0022
BR2DBP    0021
BR2T1     1000
BR2T1A    1025
BR2T1C    1074
BR2T1D    1064
BR2T1E    1015
CHNEND    0010
CLR       0002
CMDCHN    0400
CMDEND    0004
CMDHLT    0010
CMDPCK    0200
CMDRST    0040
CMDSTK    0020
CTL       6330
CTLT1     0600
CTLT2     0624
CTLT3     0662
CTLT3A    0665
CTLT4     0702
CTLT5     0735
CTLT5A    0740
CTL4A     0721
CTL4B     0725
CTL4C     0706
DEVEND    0004
INTRPT    0020
INTX      0100
```

```
INV       0004
K0377     0026
K0777     0027
K7000     0030
K7400     0031
K7767     0032
K7772     0033
RD        0001
SRVEND    0001
SRVHLT    0002
SRVPCK    0100
START     0200
STREQ     7000
TMP1      0034
TMP2      0035
TMP3      0036
TST       0002
UNCHCK    0002
WR        0004
XBIREQ    0025
XBOREQ    0024
XSRHLT    0023
```

d. Test I/O. Perform the following sequence.

    1. Place valid device address recognized by interface on BUS OUT switches.

    2. Raise ADR OUT.

    3. Raise SEL OUT. Interface will respond with OPL IN, store BUS OUT in AR1 and clear BR1, CU SEL and CMD CYC lamps will go on.

    4. Lower ADR OUT. Interface will respond with ADR IN and place AR1 on BUS IN. CU SEL lamp will go off.

    5. Raise BUS OUT (P). Lower all other BUS OUT switches. Raise CMD OUT. Interface will respond by dropping ADR IN. CMD DLY lamp will go on.

    6. Drop CMD OUT. Interface will respond with STA IN and place the status modifier bit (position 2) on BUS IN. CHL SRV lamp will come on.

    7. Raise SRV OUT. Interface will drop all inbound signals and disconnect. CMD CYC, CMD DLY, and CHL SRV lamps will all go off.

e. Start I/O. Perform the above sequence except Step 5. At Step 5 place a valid (non zero) channel command on BUS OUT and raise CMD OUT. Interface will respond by dropping ADR IN. CMD DLY lamp will go on. At Step 6 the interface will place an all-zero status byte on BUS IN. Before Step 7 press STOP on PDP-8. After Step 7 the CMD END lamp will go on CTL. Press CONTINUE; the CMD END bit will go off and the CHN REQ lamp will go on together with one or more bits in the order field of the CTL. The PDP-8 will continue running.

f. Service cycle sequences. Perform a Start I/O operation with a channel command specifying channel-inbound service (e.g., octal 2). The CHL REQ and CTL (0) lamps will go on. The REQ IN tag line lamp will also go on. Perform the following procedure.

    1. Load a nonzero device address in AR2.

2. Raise SEL OUT. Interface will respond by placing AR2 on BUS IN and raising ADR IN and OPL IN. REQ IN will be dropped. CU SEL and SRV CYC lamps will go on.

3. Lower SEL OUT. CU SEL lamp will go out.

4. Raise CMD OUT. Interface will respond by dropping ADR IN. CMD DLY lamp will go on.

5. Drop CMD OUT. Interface will respond by raising SRV IN. CHL SRV lamp will go on.

6. Stop PDP-8. Raise SRV OUT. Interface will drop all inbound tags and disconnect. SRV CYC, CMD DLY, and CHL SRV lamps will go out. BRK REQ lamp will go on.

7. Start PDP-8. The cycle will recommence at Step 2 and may be continued until either PDP-8 word count decrements to zero or until at Step 6 CMD OUT is raised instead of SRV OUT. In these cases the appropriate bits are set in CTL. (See interface description.)

222222# -163-

```
/SYSTEM/360 INTERFACE ECHO TEST ROUTINES          PAGE   1
/
/*******************************************************************
/*                                                                *
/*        SYSTEM/360 INTERFACE ECHO TEST ROUTINES                 *
/*        OR - HOW TO GET ALONG WITH THE 2870 ALMOSI              *
/*                                                                *
/*******************************************************************
/
/ASSEMBLY PARAMETERS
/
BUFSIZ=4000                   /MAXIMUM SIZE OF DATA BUFFER
/
/INTERFACE REGISTER DEFINITIONS
/
RD=1                          /IOP READ
CLR=2                         /IOP CLEAR
TST=2                         /IOP TEST
WR=4                          /IOP WRITE
INV=4                         /IOP INVERT
AR1=6300                      /ADDRESS REGISTER 1
BR1=6310                      /BUFFER REGISTER 1
AR2=6320                      /ADDRESS REGISTER 2
CTL=6330                      /CONTROL REGISTER
/
/INTERFACE CONTROL REGISTER BIT DEFINITIONS
/
STREQ=7000                    /STATUS REQUEST
BIREQ=4000                    /BUS-INBOUND SERVICE REQUEST
BOREQ=2000                    /BUS-OUTBOUND SERVICE REQUEST
CMDCHN=0400                   /COMMAND CHAIN
CMDPCK=0200                   /BUS-OUT PARITY CHECK ON COMMAND BYT
SRVPCK=0100                   /BUS-OUT PARITY CHECK ON DATA BYTE
CMDRST=0040                   /SYSTEM OR SELECTIVE RESET
CMDSTK=0020                   /STACK STATUS ON INITIAL SELECTION
CMDHLT=0010                   /HALT I/O
CMDEND=0004                   /COMMAND ACCEPT
SRVHLT=0002                   /SERVICE STOP
SRVEND=0001                   /PDP-8 WC=0
/
/SYSTEM/360 STATUS BYTE DEFINITIONS
/
UNCHCK=002                    /02 UNIT CHECK
DEVEND=004                    /04 DEVICE END
CHNEND=010                    /08 CHANNEL END
/
*2
/
BLKXFR,*.+2                   /3-CYCLE DATA BREAK BLOCK
/
*200
/
0200  4246  TEST,  JMS DELAY   /WAIT FOR CHANNEL SERVICE
0201  1320         TAD ACTIVE  /DID CHANNEL STORE COMMAND
0202  7450         SNA
0203  5200         JMP TEST    /NO. KEEP TRYING
0204  7110         CLL RAR     /YES. IS OUTBOUND SERVICE REQUESTED
0205  7620         SNL CLA
0206  5213         JMP TST2    /NO. CONTINUE
0207  1317         TAD BUFLNG  /GET BUFFER SIZE
```

```
                      /
0210   4277           JMS XMT           /YES. REQUEST OUTBOUND SERVICE
0211   2000           BOREQ
0212   5216           JMP TST3
                      /
0213   1317    TST2,  TAD BUFLNG        /GET BUFFER SIZE
0214   4277           JMS XMT           /REQUEST INBOUND SERVICE
0215   4000           BIREQ
0216   4232    TST3,  JMS STATUS        /TRANSMIT ENDING STATUS
0217   0004           DEVEND
0220   5200           JMP TEST
                      /
0221   7402    ERROR, HLT               /EQUIPMENT/PROGRAM CHECK
0222   6334           CTL INV           /RESET INTERFACE
0223   7604           LAS               /SR=ENDING STATUS
0224   7450           SNA
0225   5200           JMP TEST
0226   3230           DCA .+2
0227   4232           JMS STATUS        /TRANSMIT ENDING STATUS
0230   0000           0
0231   5200           JMP TEST          /RETURN TO WAIT LOOP
                      /
                      /TRANSMIT STATUS TO CHANNEL
                      /
0232   0000    STATUS,0                 /NORMAL ENTRY
0233   4246           JMS DELAY         /WAIT FOR CHANNEL SERVICE
0234   1312           TAD ENDCHN        /1ST BYTE - CHANNEL END
0235   3322           DCA BUF
0236   1632           TAD I STATUS      /ARGUMENT=2ND BYtE - DEVICE-END STAT
0237   2232           ISZ STATUS
0240   3323           DCA BUF+1
0241   3320           DCA ACTIVE        /RESET CHANNEL COMMAND
0242   1311           TAD K7776
0243   4277           JMS XMT           /STATUS REQUEST
0244   7000           STREQ
0245   5632           JMP I STATUS      /NORMAL EXIT
                      /
                      /DELAY FOR CHANNEL OPERATION
                      /
0246   0000    DELAY, 0                 /NORMAL ENTRY
0247   6331           CTL RD            /READ INTERFACE STATUS
0250   3321           DCA TMP
0251   1321           TAD TMP           /IS INTERFACE BUSY
0252   0310           AND K7000
0253   7640           SZA CLA
0254   5247           JMP DELAY+1       /YES. CONTINUE IN WAIT LOOP
0255   1321           TAD TMP           /NO. HAS DEVICE ADDRESS BEEN STORED
0256   0315           AND CMDBIT
0257   7650           SNA CLA
0260   5266           JMP DEL1          /NO. CONTINUE
0261   6301           AR1 RD            /YES. COPY AR1 IN AR2
0262   6326           AR2 CLR+WR
0263   7200           CLA
0264   6311           BR1 RD            /STORE CHANNEL COMMAND
0265   3320           DCA ACTIVE
0266   1321    DEL1,  TAD TMP           /RESET INTERFACE
0267   0314           AND RSTBIT
0270   6334           CTL INV
0271   7200           CLA
```

```
                 /
0272   1321          TAD TMP            /ARE ANY UNUSUAL-END BITS SET
0273   0313          AND BADBIT
0274   7450          SNA
0275   5646          JMP I DELAY        /NO. NORMAL EXIT
0276   5221          JMP ERROR          /YES. ABORT
                 /
                 /TRANSMIT BYTES ON MULTIPLEX CHANNEL
                 /
0277   0000  XMT,    0                  /ENTRY. AC=WC
0300   3002          DCA BLKXFR
0301   1316          TAD PTR
0302   3003          DCA BLKXFR+1
0303   1677          TAD I XMT          /ARGUMENT=CTL BITS
0304   2277          ISZ XMT
0305   6334          CTL INV            /START OPERATION
0306   7200          CLA
0307   5677          JMP I XMT          /NORMAL EXIT
                 /
0310   7000  K7000,  7000
0311   7776  K7776,  7776
0312   0010  ENDCHN,CHNEND
0313   0370  BADBIT,CMDRST+CMDSTK+CMDHLT+CMDPCK+SRVPCK
0314   0407  RSTBIT,CMDEND+SRVEND+SRVHLT+CMDCHN
0315   0034  CMDBIT,CMDSTK+CMDHLT+CMDEND
0316   0321  PTR,    BUF-1              /POINTER FOR DATA BREAK
0317   4000  BUFLNG,-BUFSIZ             /BUFFER SIZE
0320   0000  ACTIVE,0                   /CHANNEL COMMAND
             TMP,    *.+1               /TEMPORARY
             BUF,    *.+BUFSIZ          /BUFFER
                 /
ACTIVE   0320
AR1      6300
AR2      6320
BADBIT   0313
BIREQ    4000
BLKXFR   0002
BOREQ    2000
BR1      6310
BUF      0322
BUFLNG   0317
BUFSIZ   4000
CHNEND   0010
CLR      0002
CMDBIT   0315
CMDCHN   0400
CMDEND   0004
CMDHLT   0010
CMDPCK   0200
CMDRST   0040
CMDSTK   0020
CTL      6330
DELAY    0246
DEL1     0266
DEVEND   0004
ENDCHN   0312
ERROR    0221
INV      0004
K7000    0310
```

```
K7776     0311
PTR       0316
RD        0001
RSTBIT    0314
SRVEND    0001
SRVHLT    0002
SRVPCK    0100
STATUS    0232
STREQ     7000
TEST      0200
TMP       0321
TST       0002
TST2      0213
TST3      0216
UNCHCK    0002
WR        0004
XMT       0277
```

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)*	2a. REPORT SECURITY CLASSIFICATION
THE UNIVERSITY OF MICHIGAN CONCOMP PROJECT	Unclassified
	2b. GROUP

3. REPORT TITLE

SYSTEM/360 INTERFACE ENGINEERING REPORT

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*
Memorandum 13

5. AUTHOR(S) *(First name, middle initial, last name)*

MILLS, DAVID

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
March, 1968	166	none
8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)	
DA-49-083 OSA-3050	Memorandum 13	
b. PROJECT NO.		
c.	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*	
d.		

10. DISTRIBUTION STATEMENT

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11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY

13. ABSTRACT

An interface which connects a small special-purpose digital computer to a large general-purpose digital data processing system is described in this report. The small computer is the Digital Equipment Corporation PDP-8 which itself is a component of a data collection and distribution system called the Data Concentrator. The large data processing system is the IBM System/360 Model 67, which is the principal computing element at The University of Michigan Computing Center. The interface is designed to be attached to the multiplexor channel of the Model 67 along with other input-output components such as card readers, line printers, and communications equipment, and satisfies all IBM standards and interface conventions established for this type of attachment. The interface provides a bidirectional data transfer between the two machines of up to 80 thousand bytes (characters) per second using cycle-steal techniques in which data are transferred directly between the Model 67 multiplexor channel and the PDP-8 core memory without explicit program intervention.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
interface, multiplexor channel, cycle-steal, control unit, PDP-8, System/360, Model 67, data transmission,						
	ROLE	WT	ROLE	WT	ROLE	WT